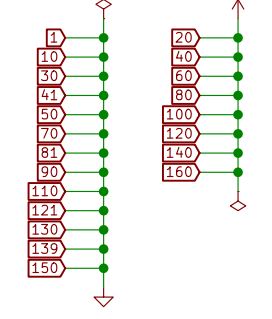
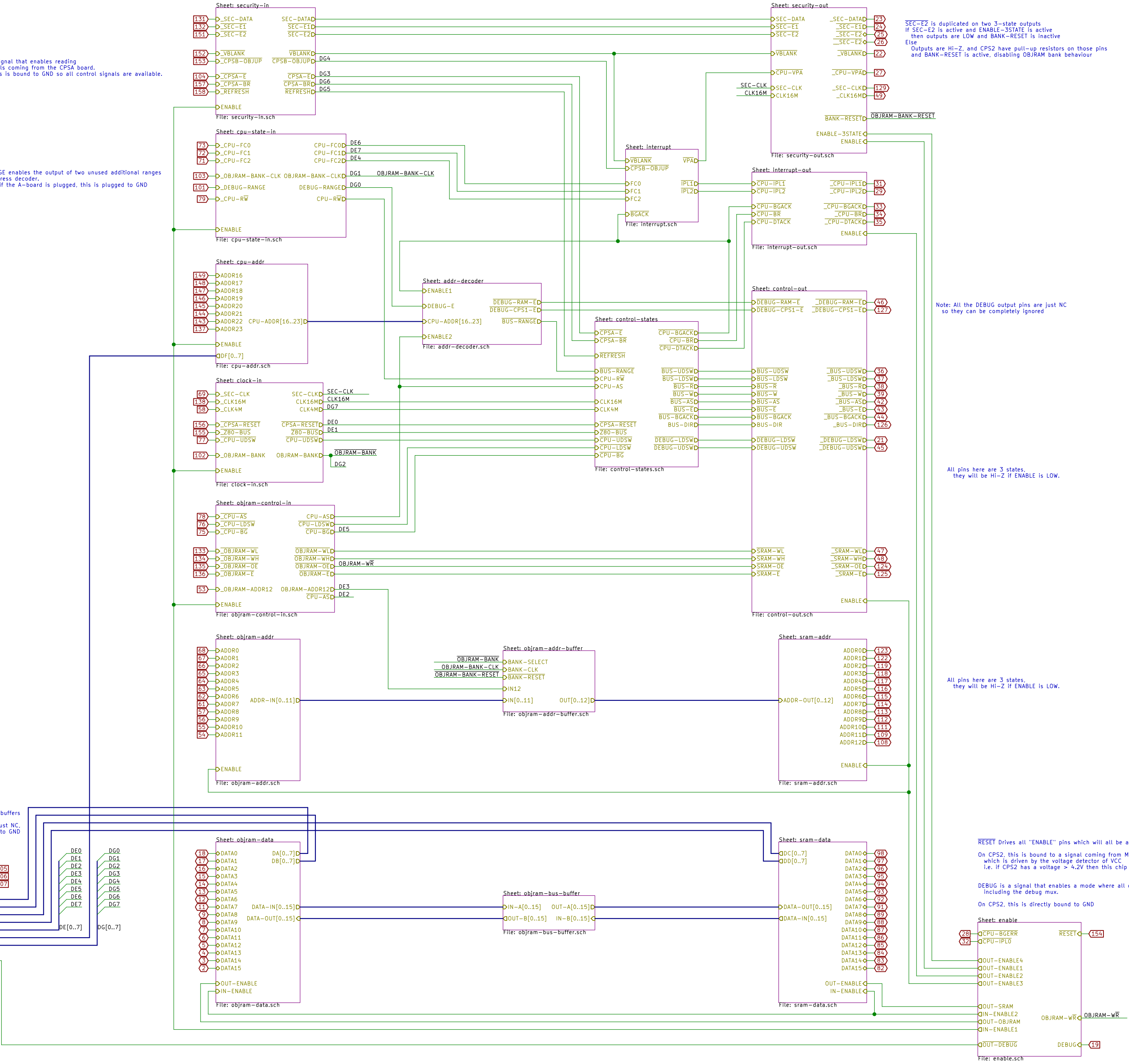
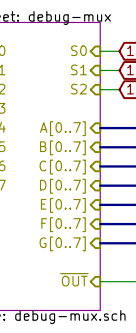


CPSA-E is a signal that enables reading control signals coming from the CPSA board. On CPS2, this is bound to GND so all control signals are available.

DEBUG-RANGE enables the output of two unused additional ranges of the address decoder. On CPS2, if the A-board is plugged, this is plugged to GND



This bus multiplexer is a way to see various inputs after buffers. On CPS2, the output is not enabled so pins are just NC, also S0-S2 are bound to GND



SEC-E2 is duplicated on two 3-state outputs. If SEC-E2 is active and ENABLE-3STATE is active then outputs are LOW and BANK-RESET is inactive. Else outputs are Hi-Z, and CPS2 have pull-up resistors on those pins and BANK-RESET is active, disabling OBJRAM bank behaviour.

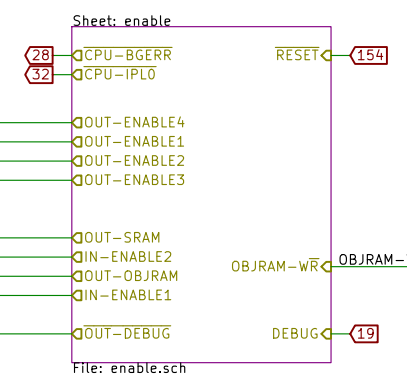
Note: All the DEBUG output pins are just NC so they can be completely ignored

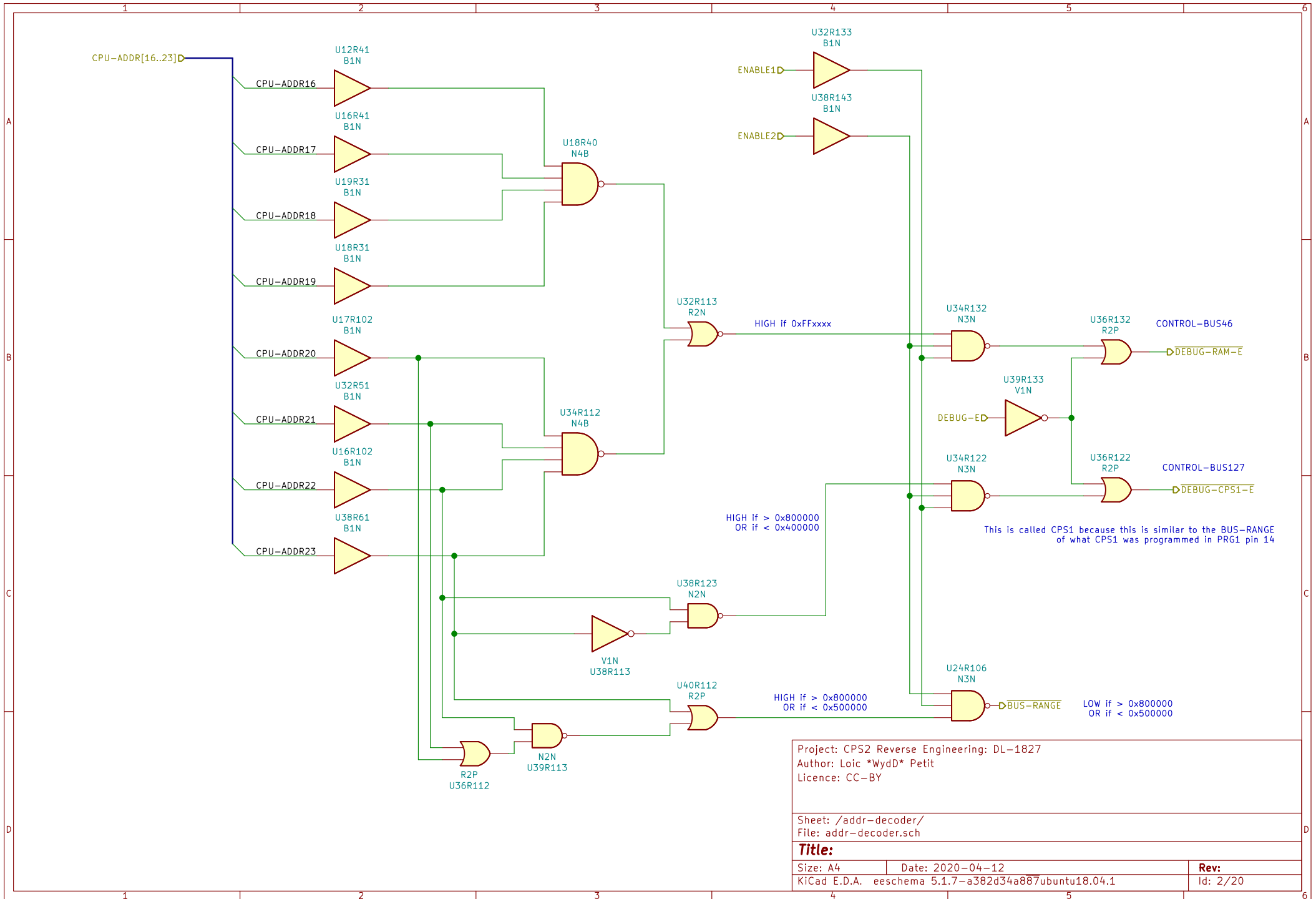
All pins here are 3 states, they will be Hi-Z if ENABLE is LOW.

All pins here are 3 states, they will be Hi-Z if ENABLE is LOW.

RESET Drives all "ENABLE" pins which will all be active if RESET is inactive. On CPS2, this is bound to a signal coming from MIF which is driven by the voltage detector of VCC. i.e. if CPS2 has a voltage > 4.2V then this chip will work as intended.

DEBUG is a signal that enables a mode where all outputs are enabled including the debug mux. On CPS2, this is directly bound to GND





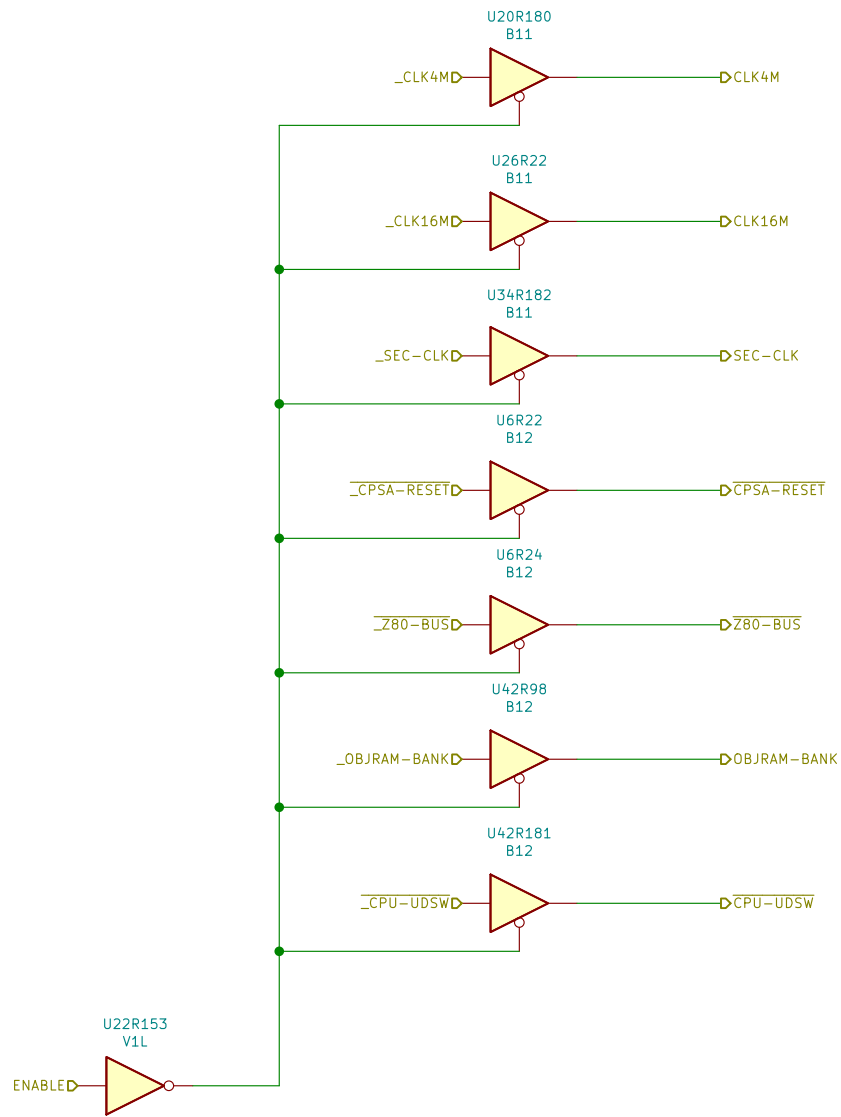
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

Sheet: /addr-decoder/
 File: addr-decoder.sch

Title:

Size: A4 Date: 2020-04-12
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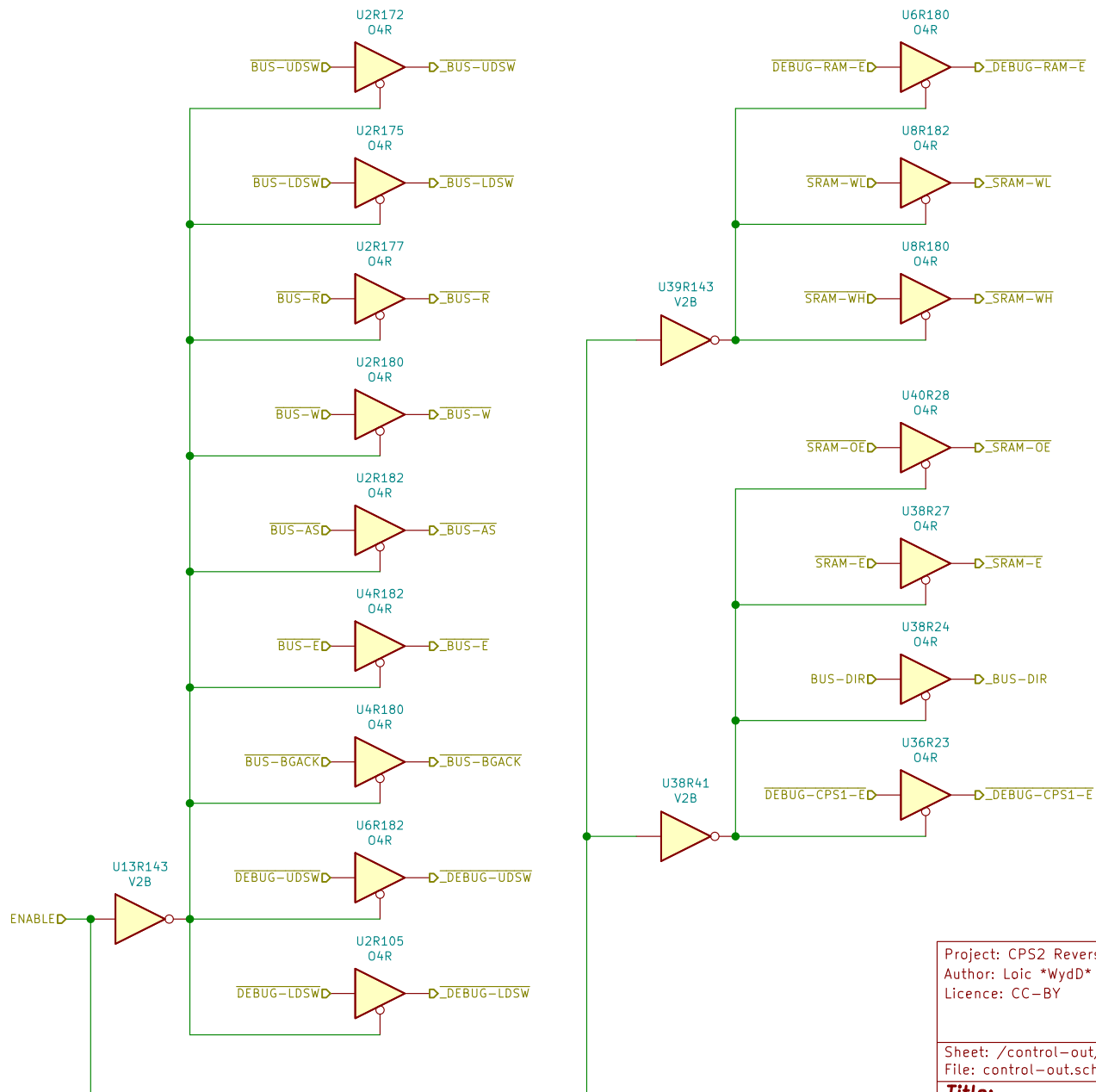
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

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 KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1

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 Id: 3/20



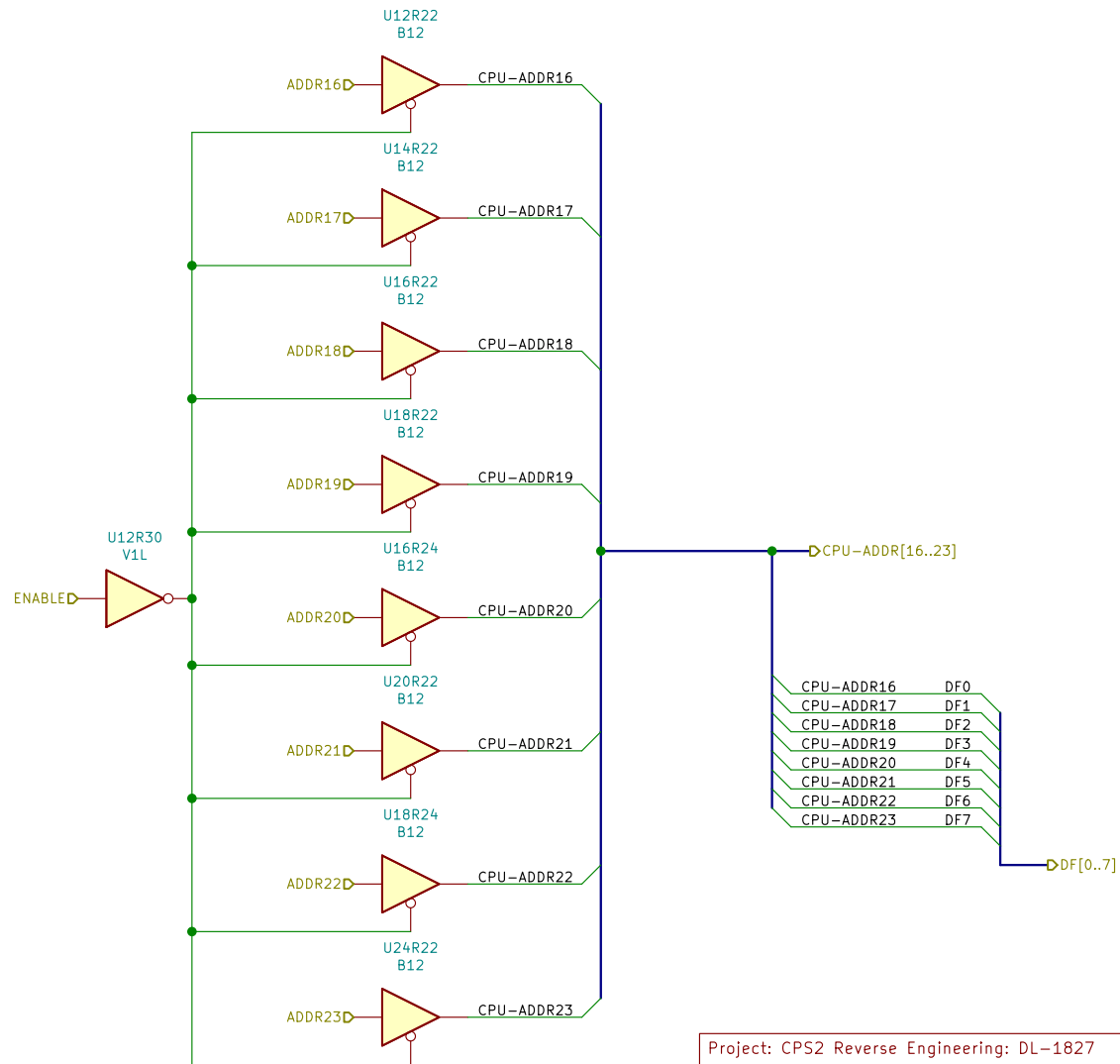
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

Sheet: /control-out/
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 Id: 4/20



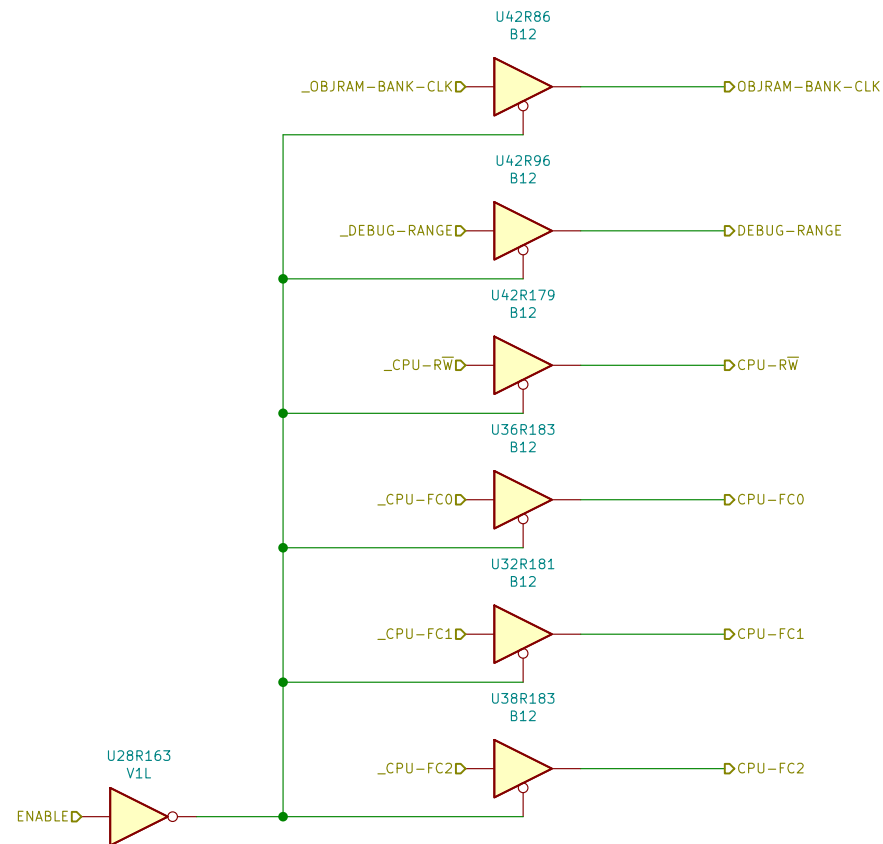
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *Wyd* Petit
 Licence: CC-BY

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 Id: 6/20



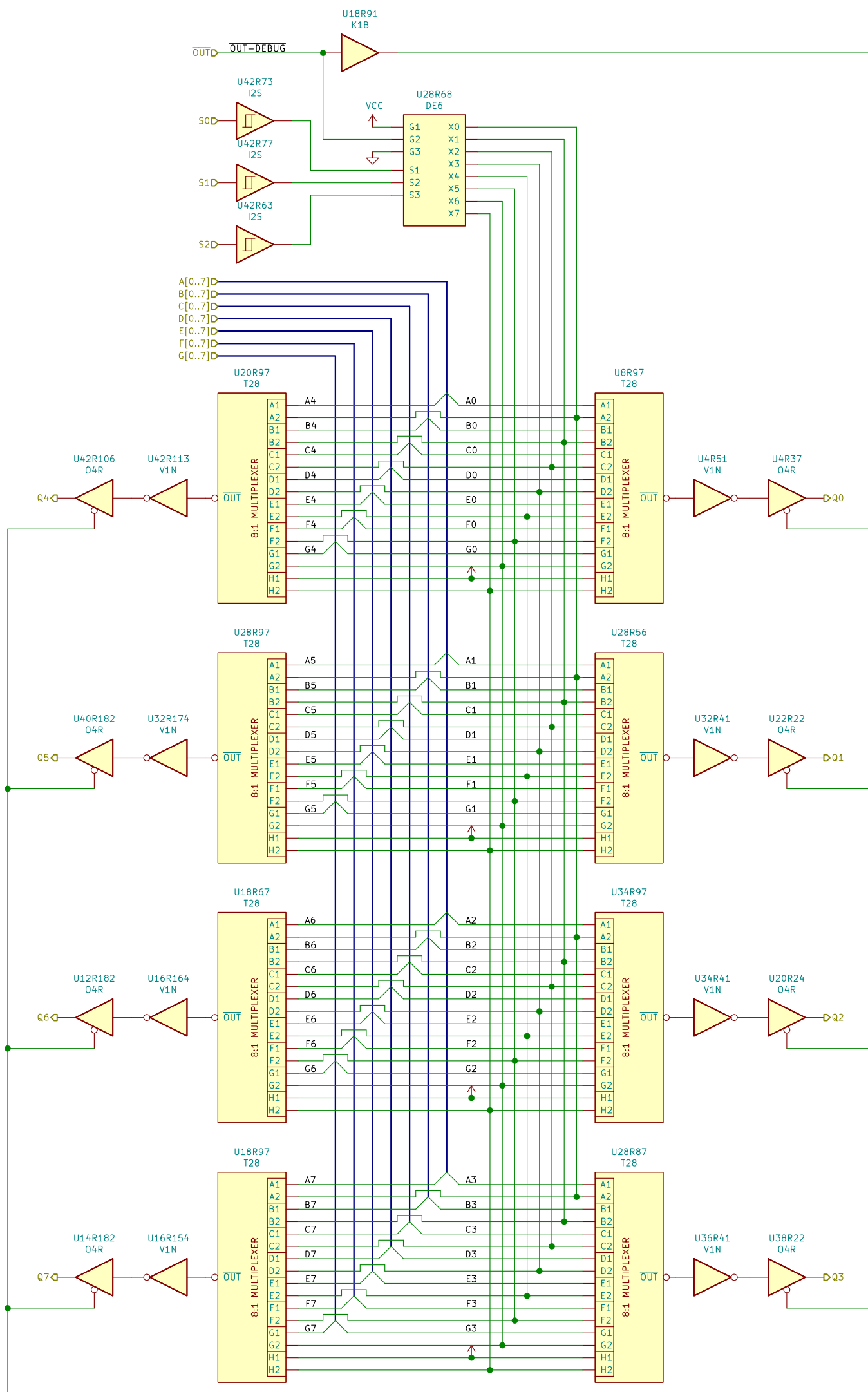
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

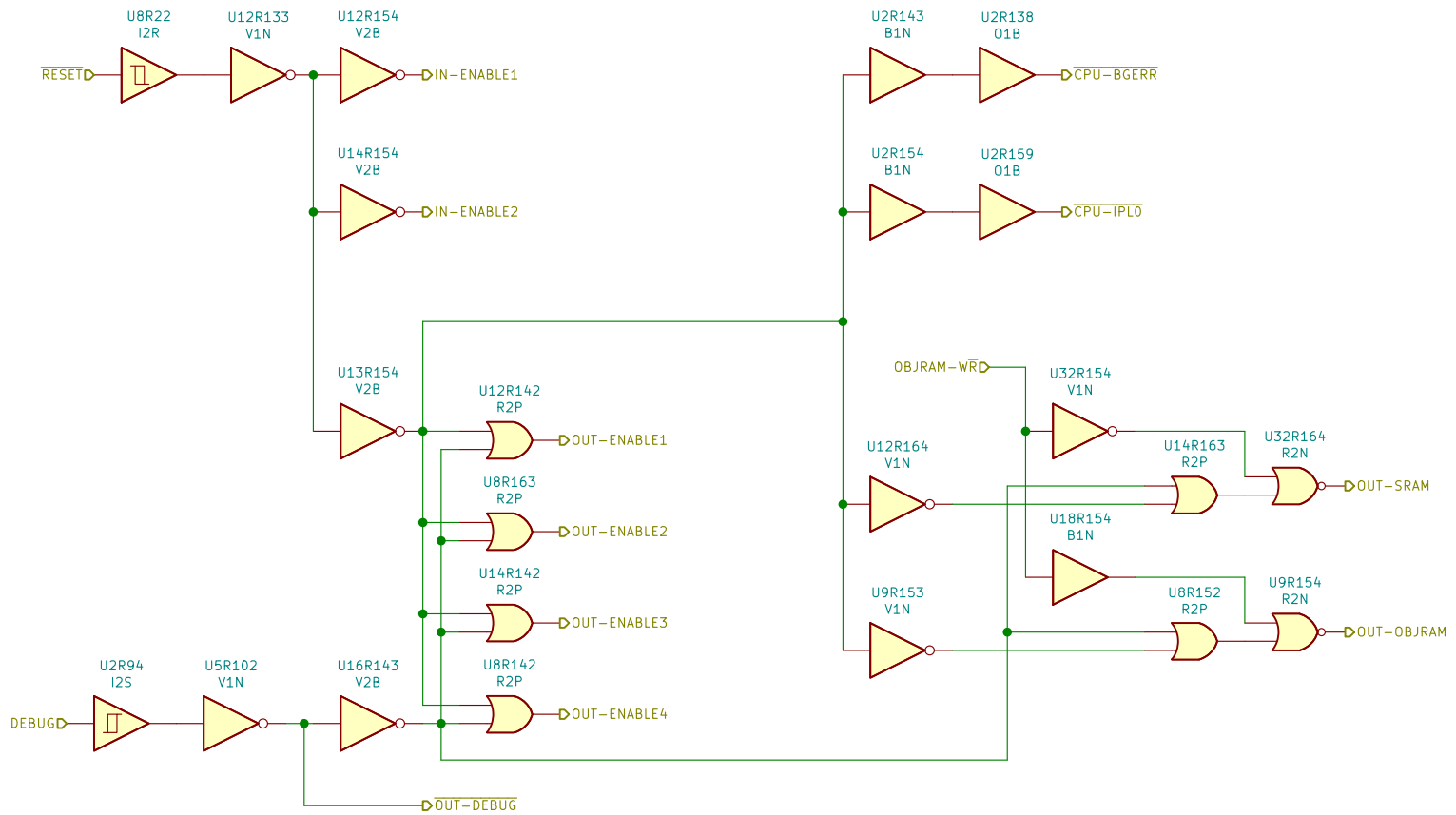
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 Id: 7/20





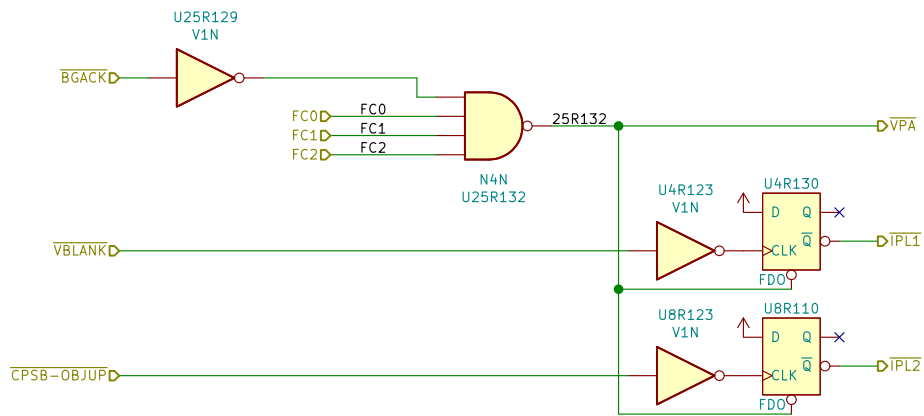
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

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 Id: 9/20



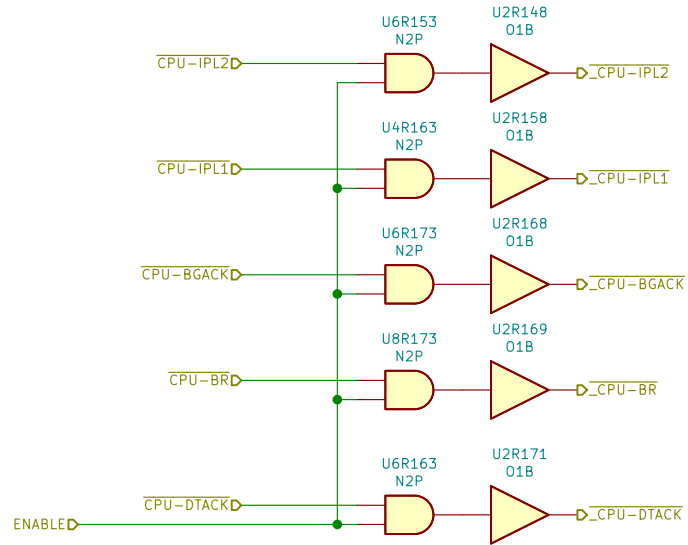
Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

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Size: A4 Date: 2020-04-12
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 Id: 10/20



Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
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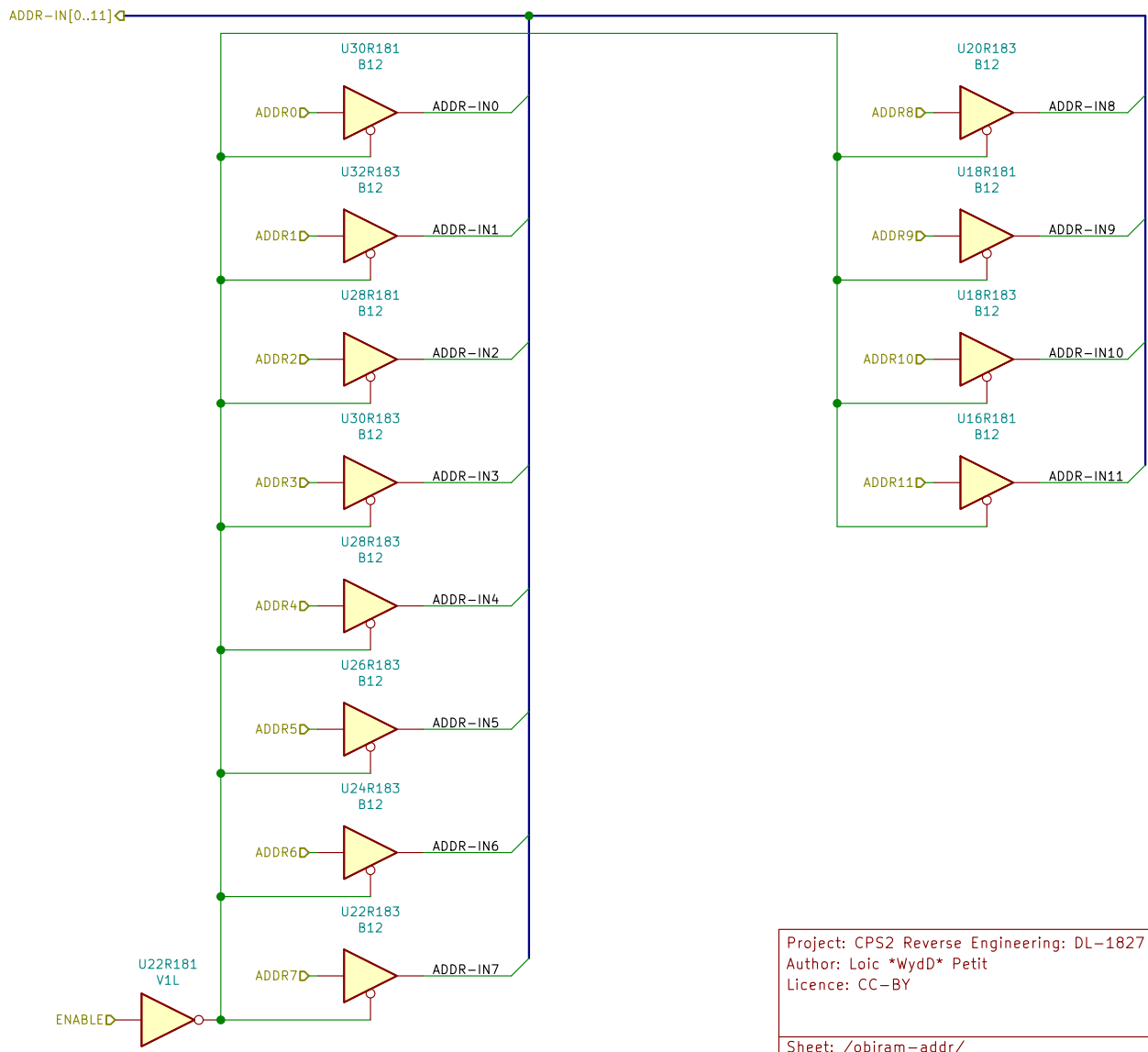
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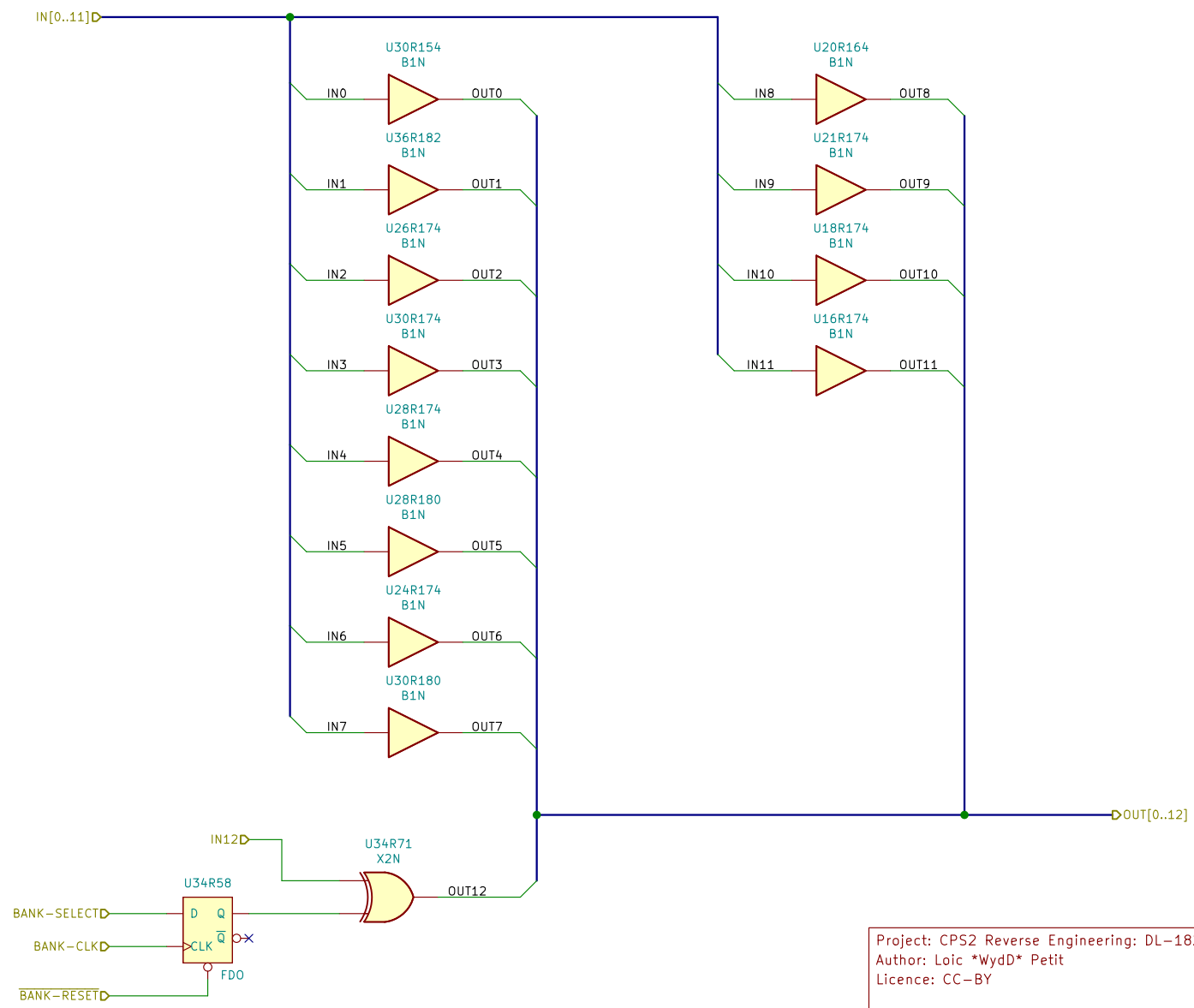
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Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *Wyd* Petit
 Licence: CC-BY

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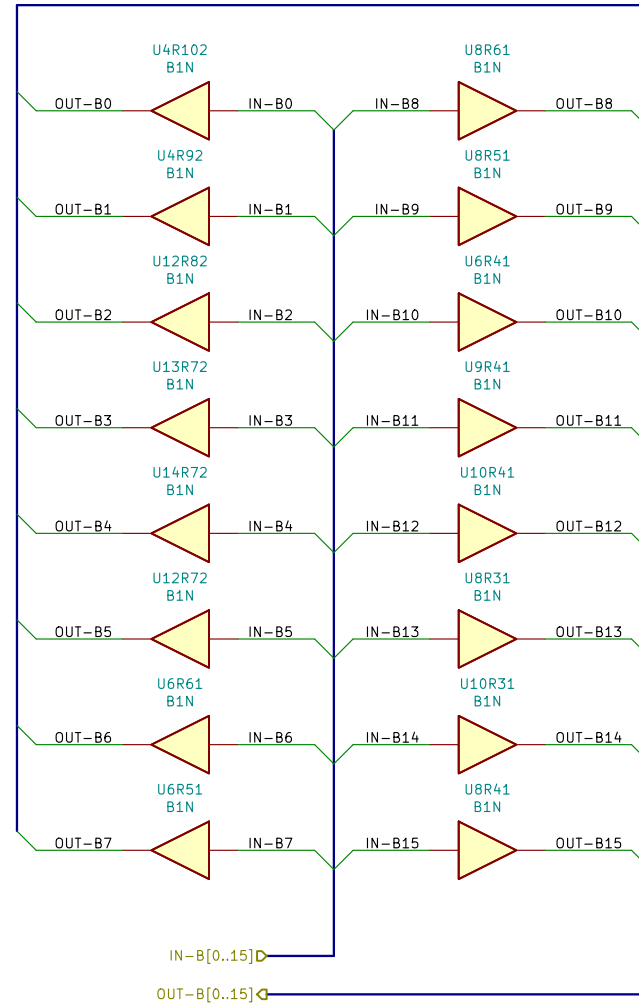
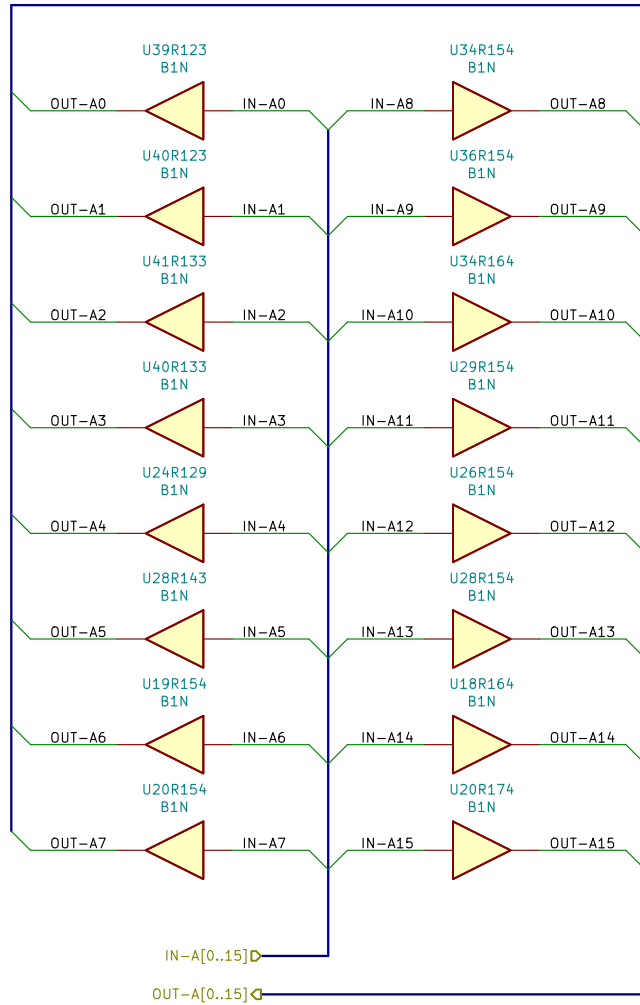
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Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
 Licence: CC-BY

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Rev: Id: 13/20	



Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *Wyd* Petit
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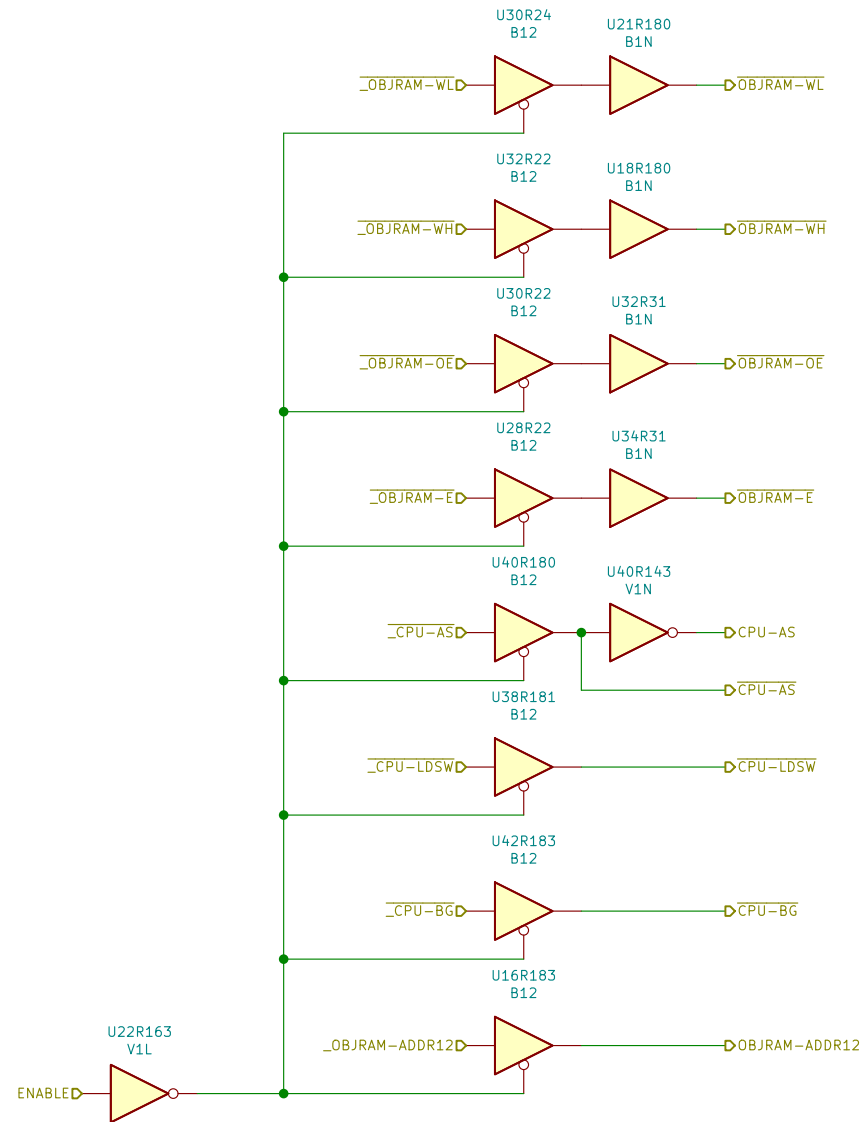
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Date: 2020-04-12

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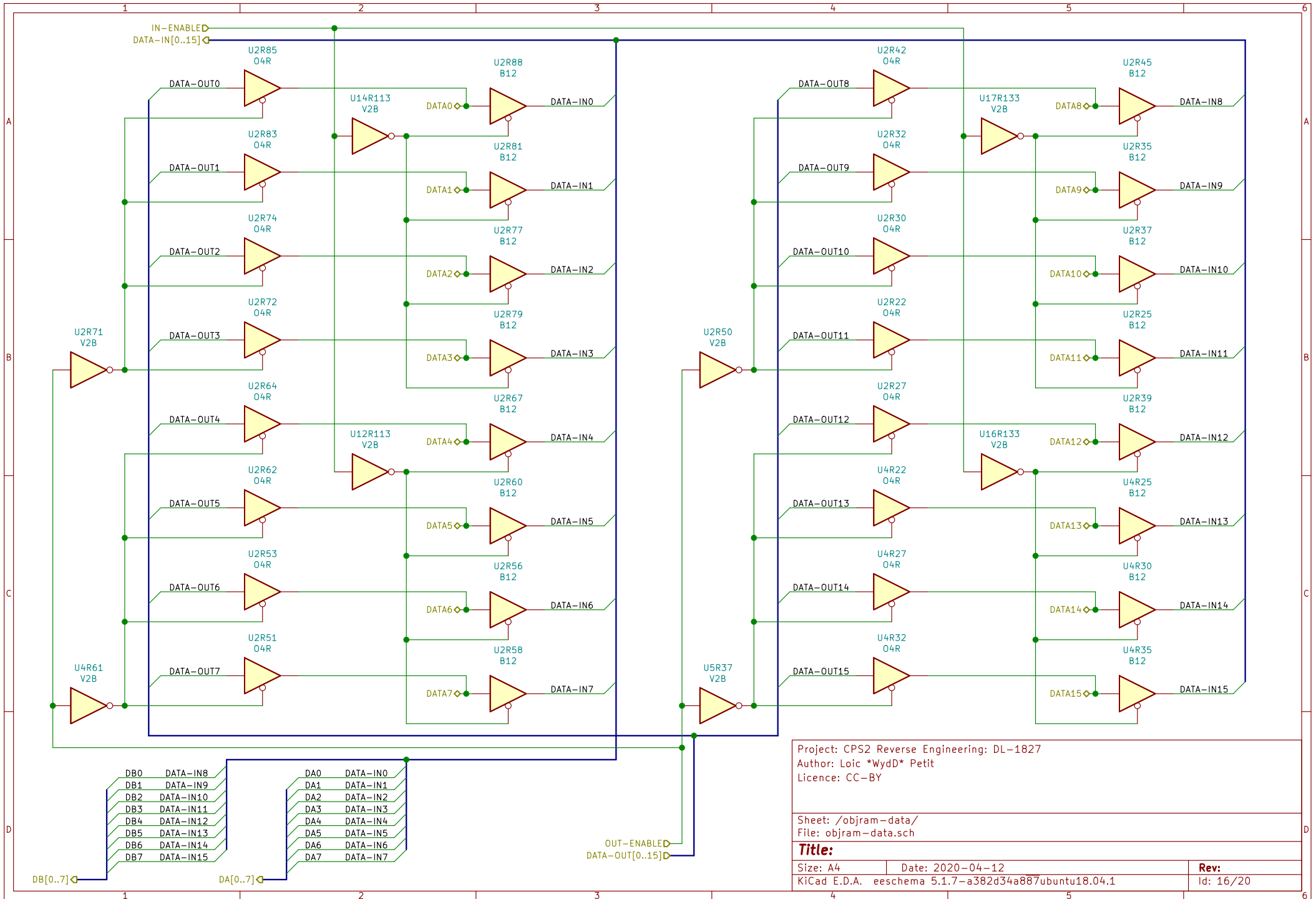
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 Author: Loic *WydD* Petit
 Licence: CC-BY

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Size: A4 Date: 2020-04-12
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Project: CPS2 Reverse Engineering: DL-1827
 Author: Loic *WydD* Petit
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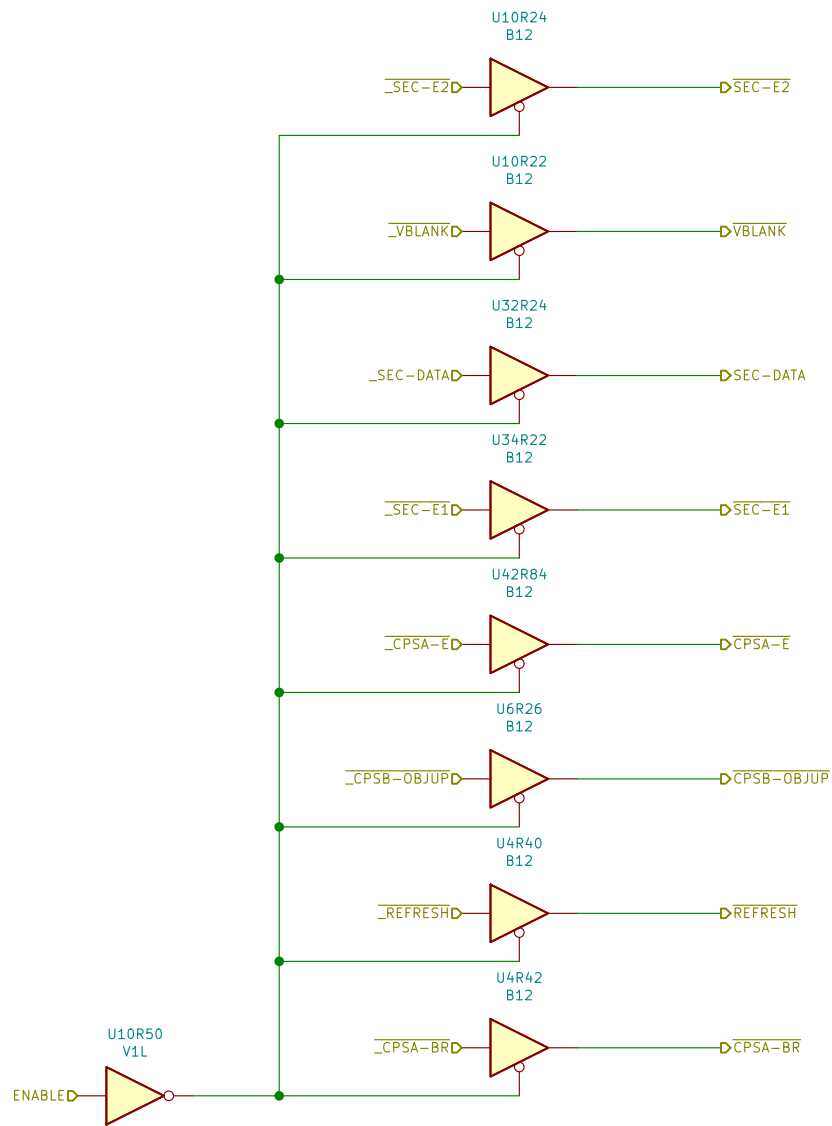
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Date: 2020-04-12

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 Id: 16/20



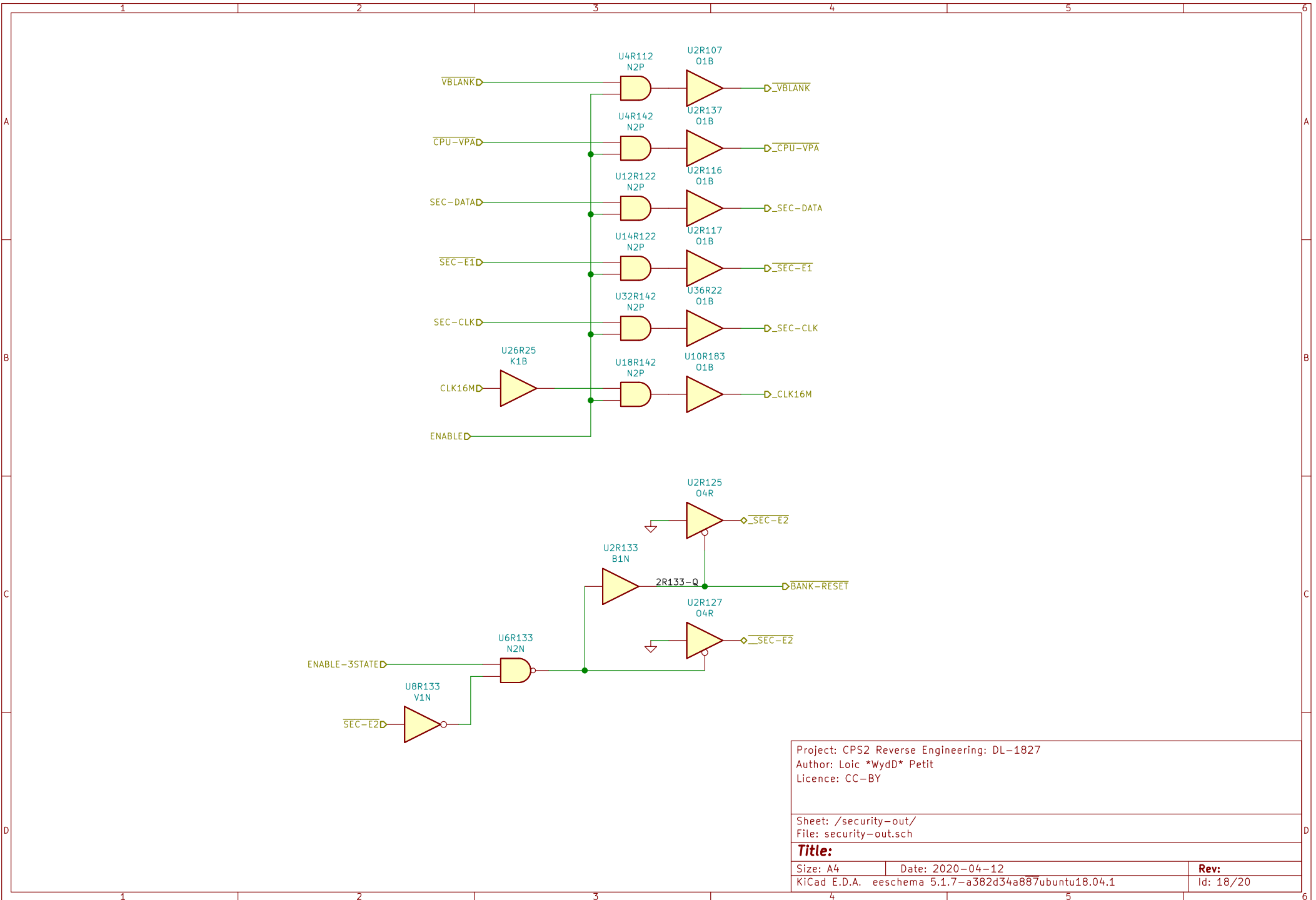
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 Author: Loic *WydD* Petit
 Licence: CC-BY

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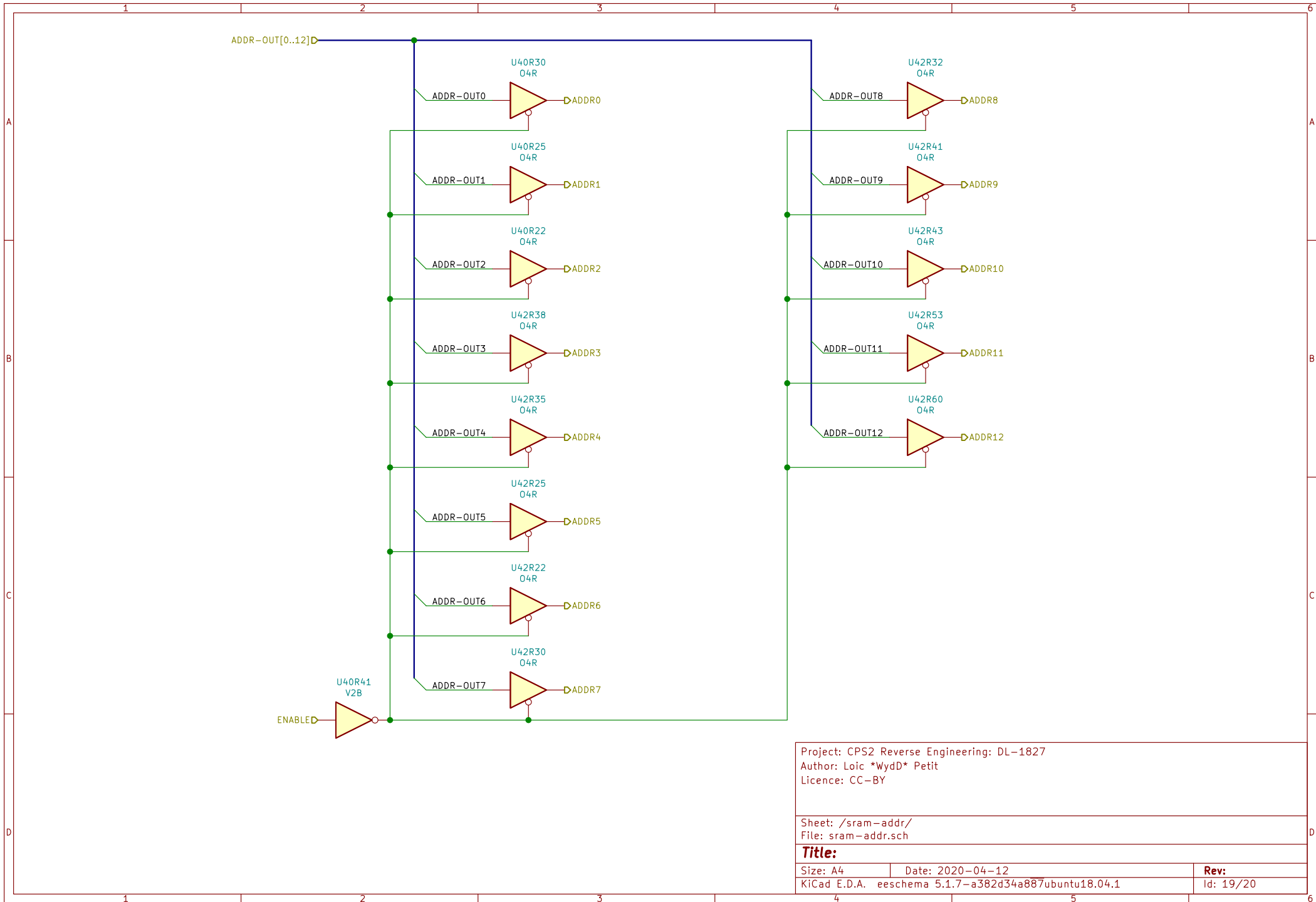
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 Author: Loic *WydD* Petit
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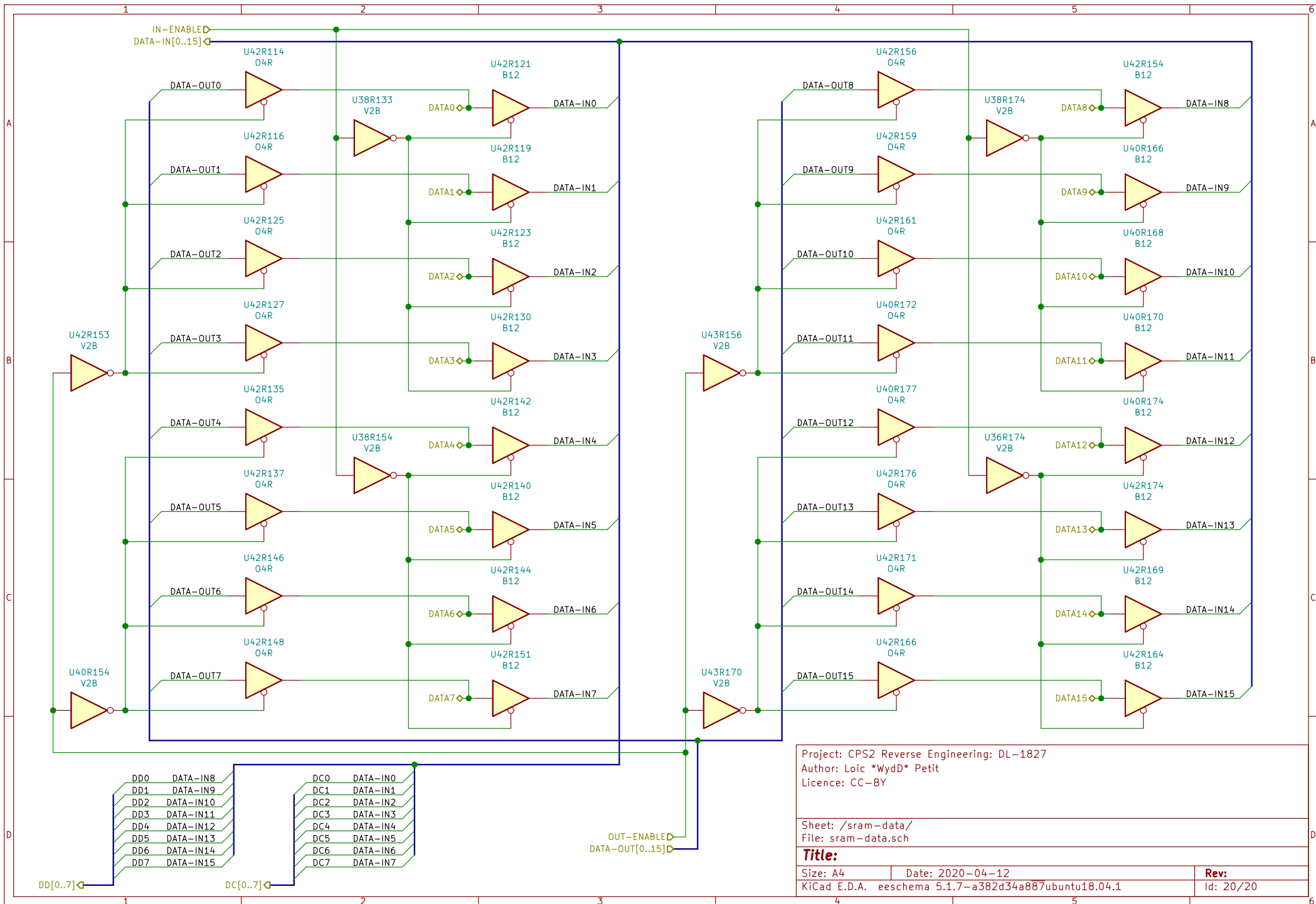
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