

This unused I/O is a 3bit decoder.
 Say if 011 is the input of S[0..2], all outputs will be Hi-Z except pin 153 (= 3)
 On CPS2 those are just bound to a pull-up resistor array.
 The state of this IO can be read using the REG8 address.
 MSB will contain the S[0..2] data

ENABLE-ADDR is C25 on CN3. When A-board is connected it is HIGH.
 It controls the permission to transmit the ADDR bus and enable transceivers.
 A-BOARD-CONNECTED is C26 on CN3 when the A-board is connected it is LOW.
 Useless in normal operations. If ENABLE-ADDR is low, controls the direction of the data.
 ENABLE-DATA is connected to PAL B2 which control if data output is available.
 Typically used to exclude OBJRAM range

VCC-OK is connected to a voltage detector on VCC
 It's HIGH if VCC is above 4.2V
 The RESET signal will distribute HIGH to all DLs on CPS2
 Signals are shown assuming CPS2 wiring (DEBUG excluded)

Sheet: enable
 56 VCC-OK
 66 RESET
 HIGH ENABLE-ADDR
 35 DEBUG

ENABLE-ADDR
 ADDR-BUS-HI
 ADDR-BUS-LO
 ENABLE-ADDR-OUT

ENABLE1 LOW if DEBUG
 ENABLE2 LOW if DEBUG
 ENABLE3 LOW if DEBUG

IN-ENABLE HIGH
 ENABLE-CLK HIGH

OUT-DEBUG DEBUG

File: enable.sch

DEBUG is connected to GND on the actual CPS2,
 it is surely connected to other things on the dev board

The core contains 8 bits of registers.
 They can be written on using the bus,
 hence the presence of an address decoding logic.
 Read operations may not read the registers by itself.

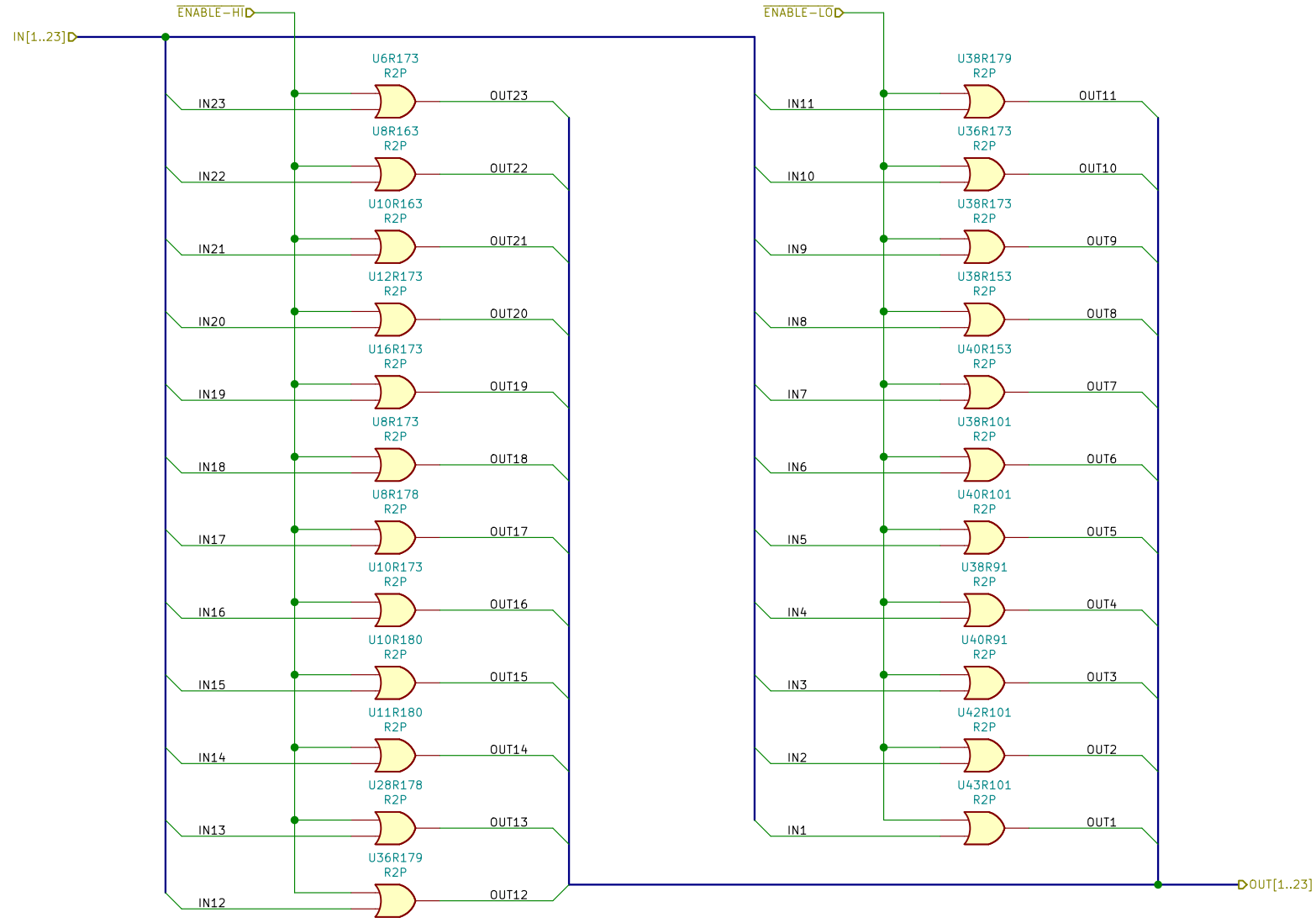
The (simplified) range is 0x804xxx
 - 08x [rw]: 1bit on pin 147, read is muxed on the bus (see notes)
 - 09x [rw]: 5+1 bits of reg, read is muxed on the bus (see notes)
 - 0Ax [w]: 1bit, changes the behaviour of the bus (see notes)
 - 0Bx [r]: empty, read signal redirected outside via pin 46 (NC)
 - 0Ex [w]: Objram bank selection, signal transmitted to the CIF

REG9 is unused on the CPS2
 they are only connected to a pull-up resistor array
 It is split in two. LSB[0..4] and MSB[15]
 It is possible to override the bus content by setting REGA to 1
 It will override the output of REG9 internal value using the pins as input.
 By default the value of this register is 0 except for the MSB

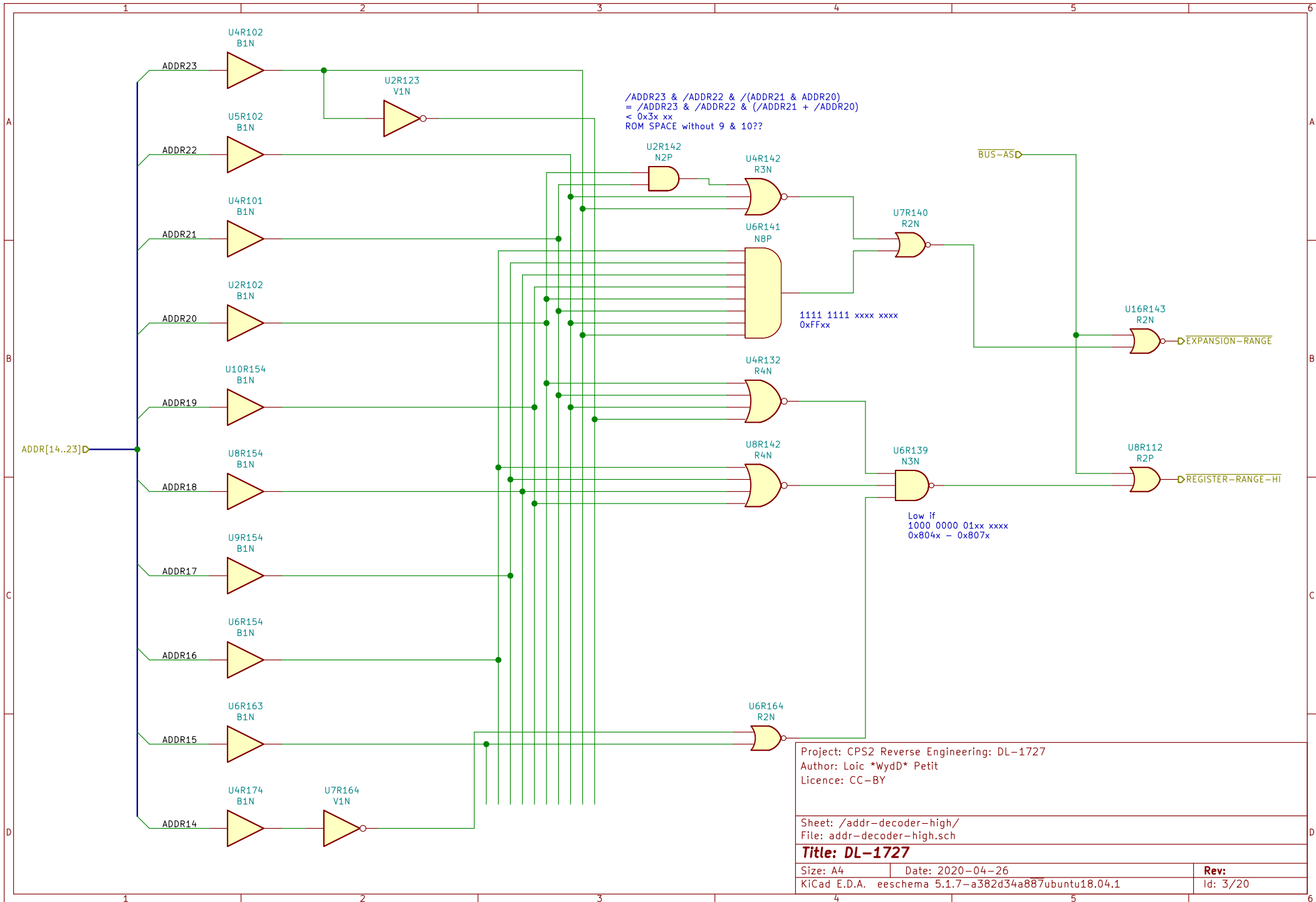
This debug multiplexer is a way to see various inputs after buffers.
 On CPS2, the output is disabled, pins are NC and input pins are bound to GND

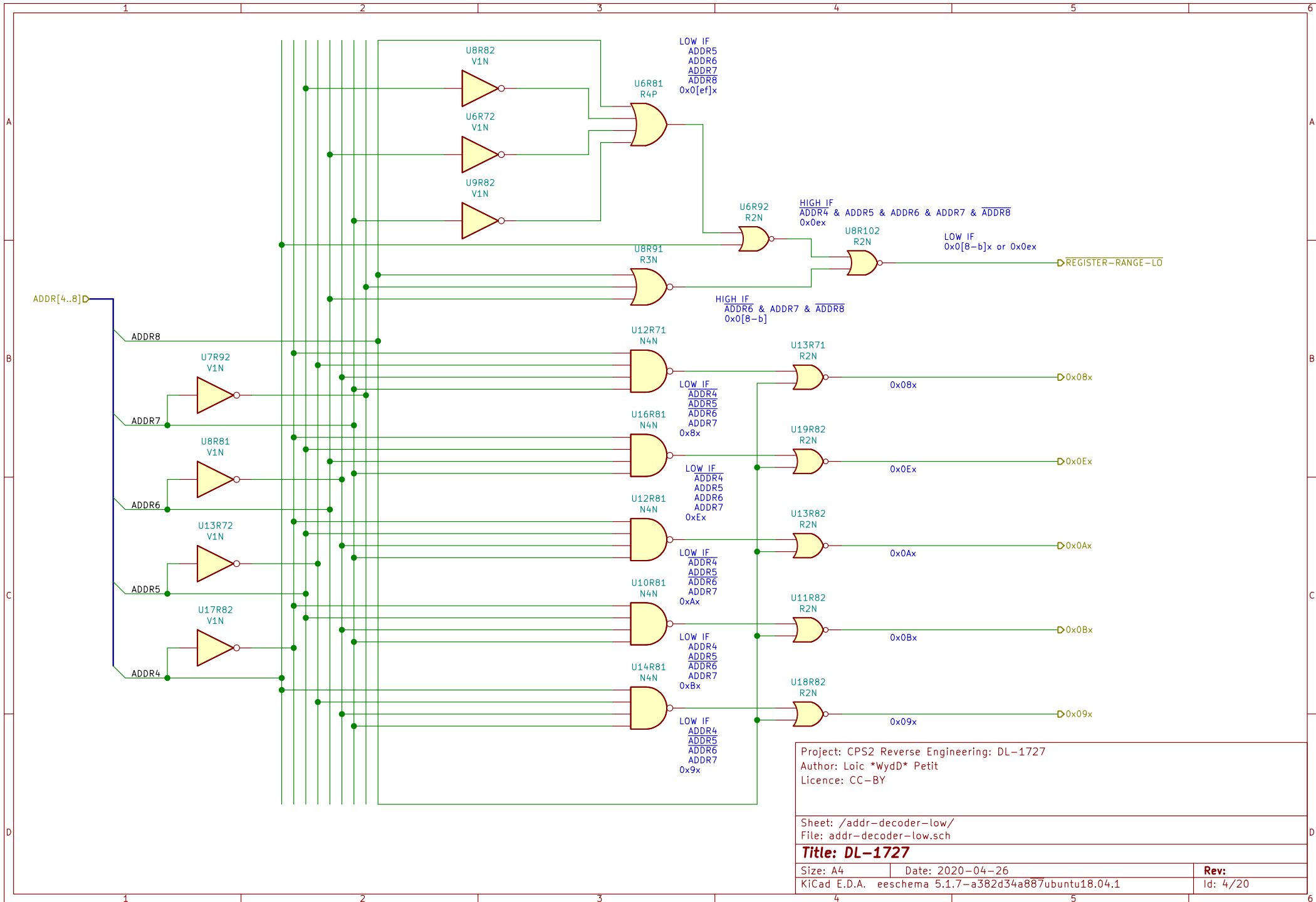
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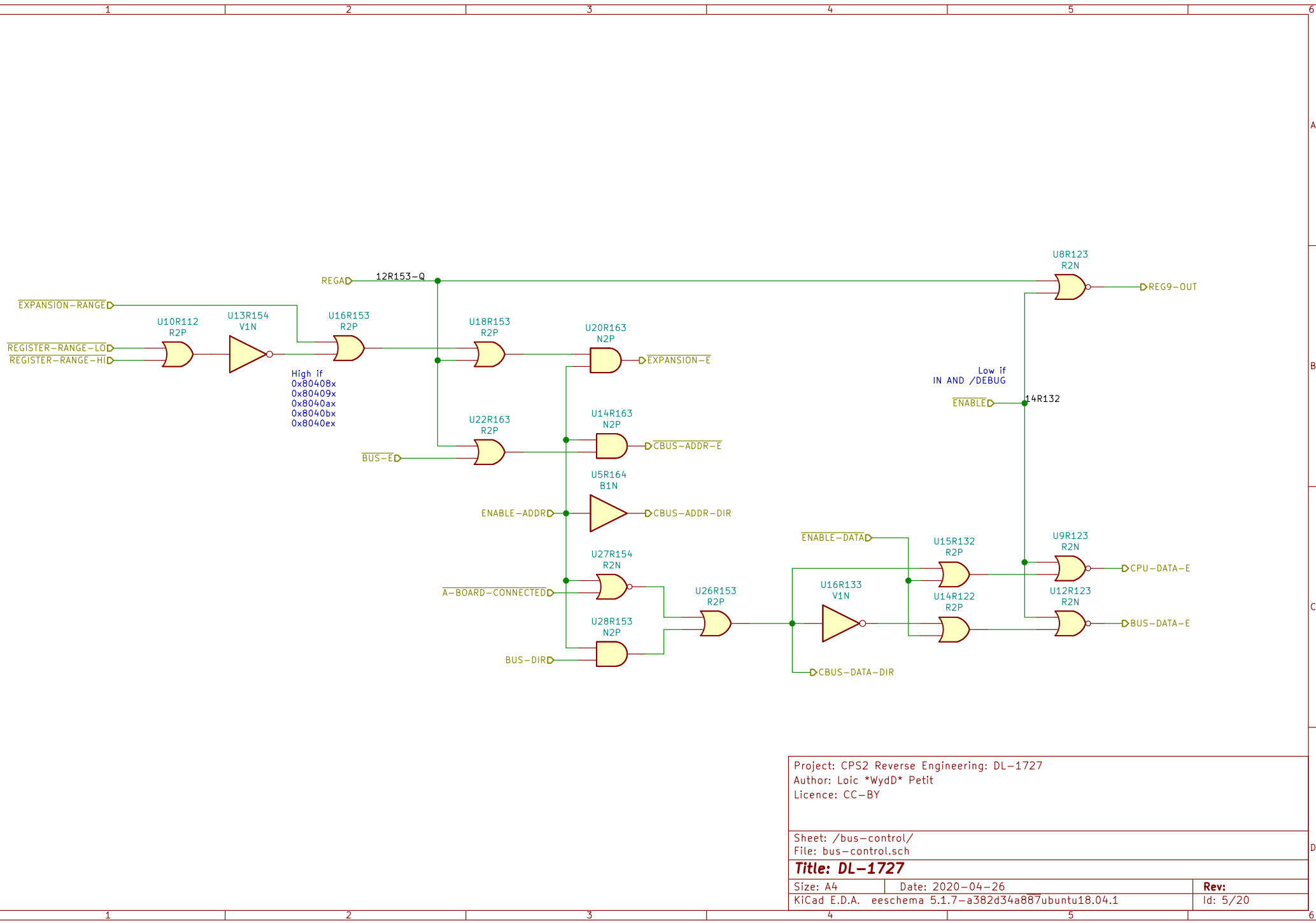
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Title: DL-1727
 Size: A3 Date: 2020-04-26 Rev:
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Sheet: /addr-bus-enable/	
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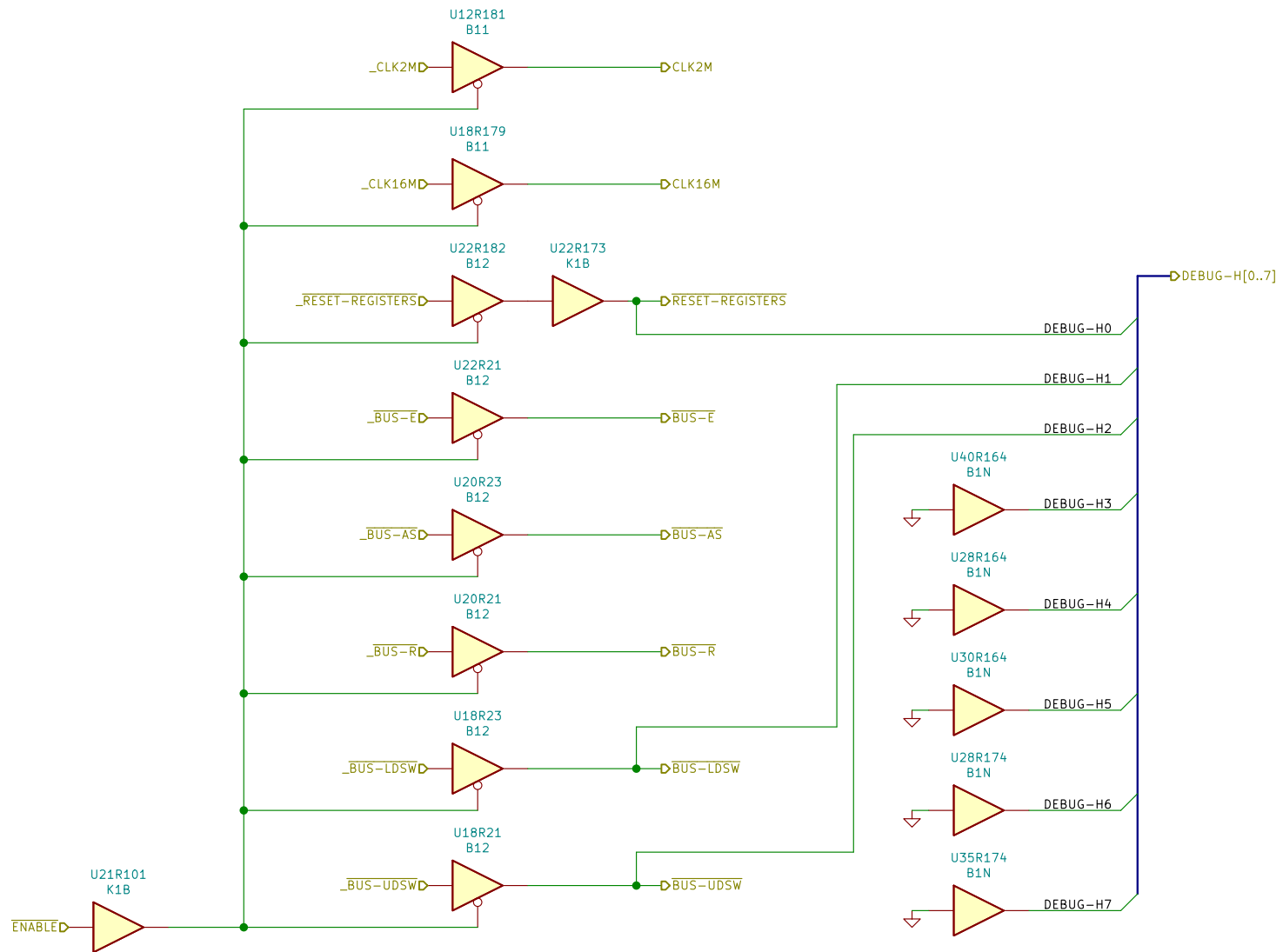


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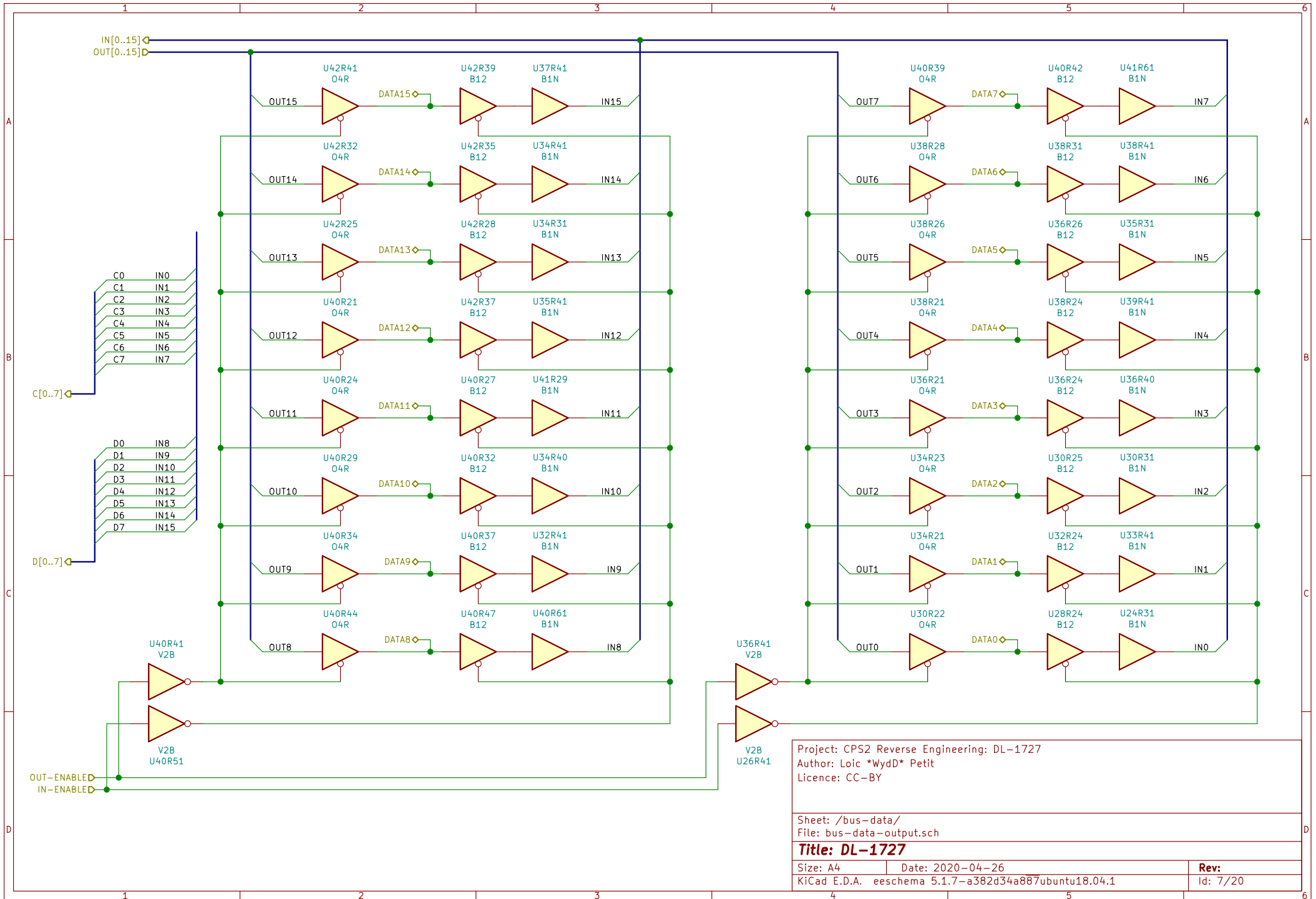
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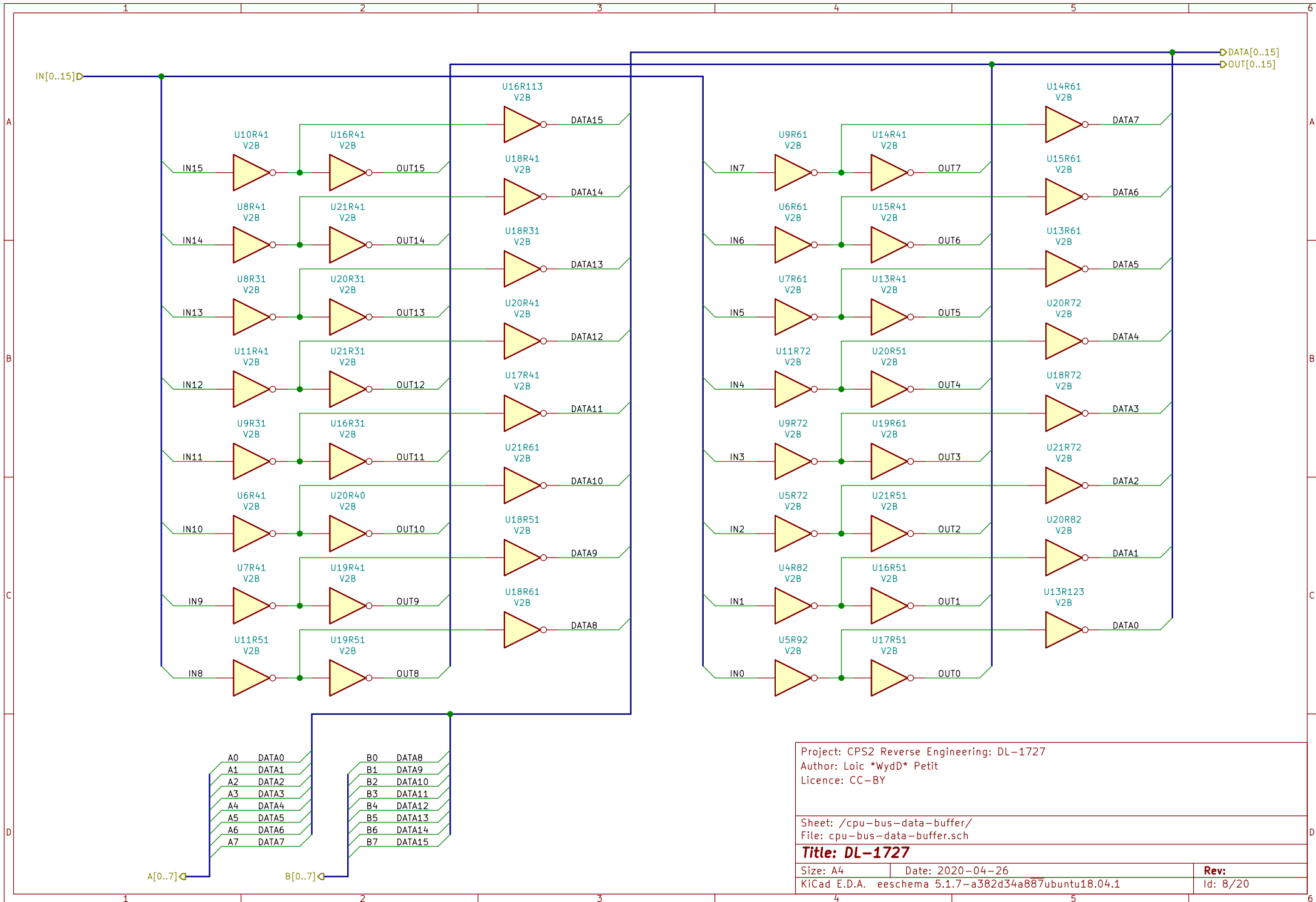
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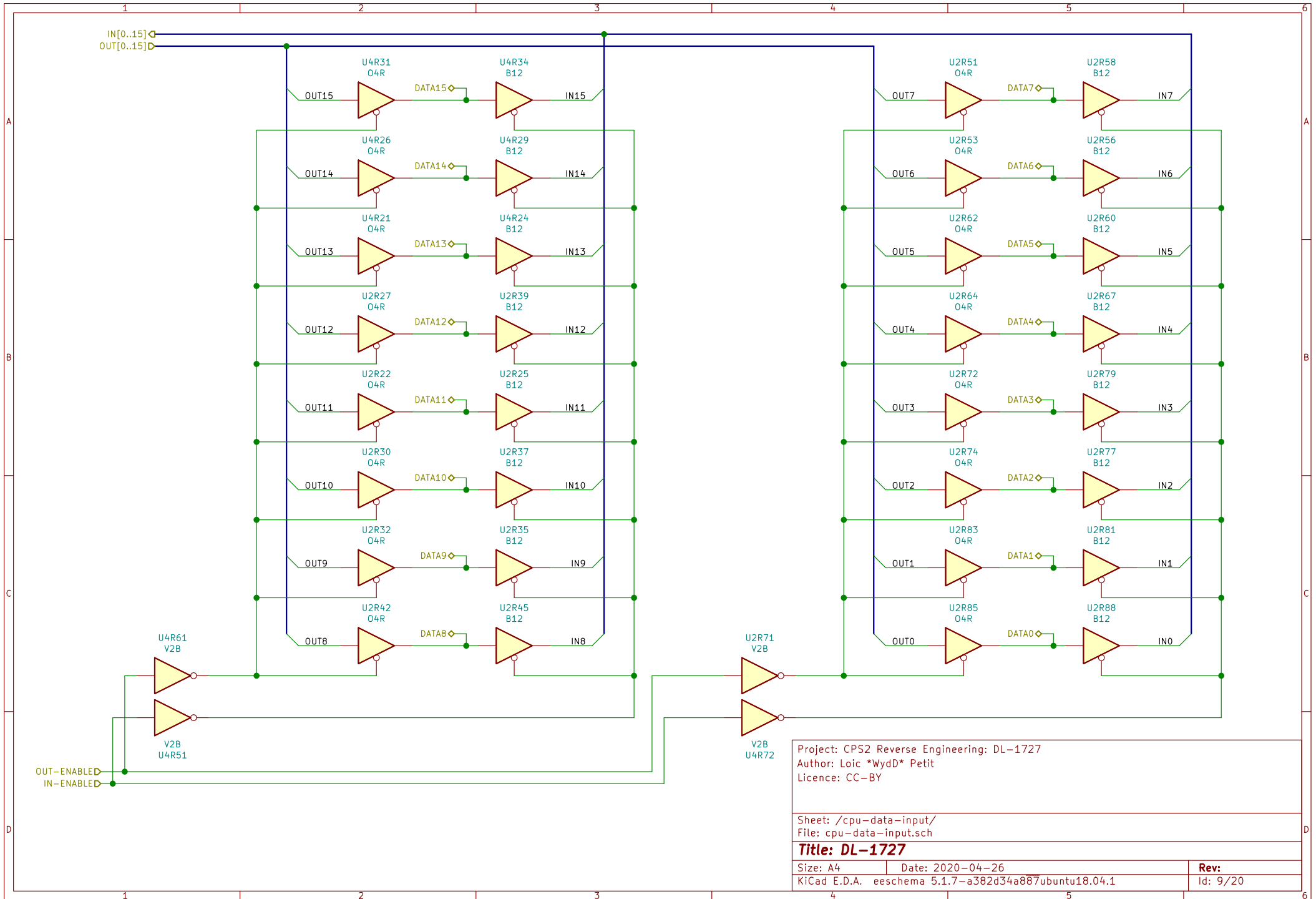
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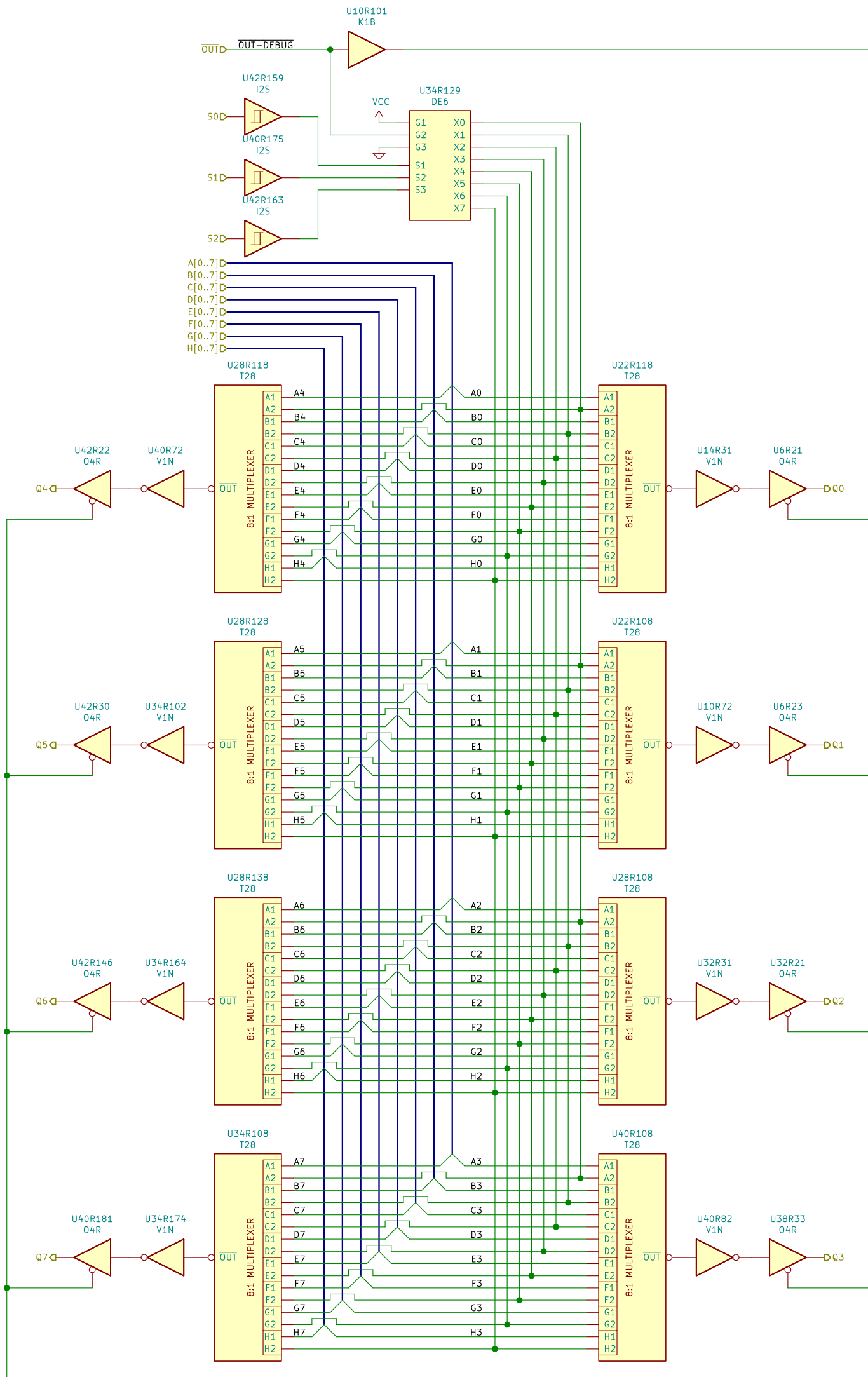
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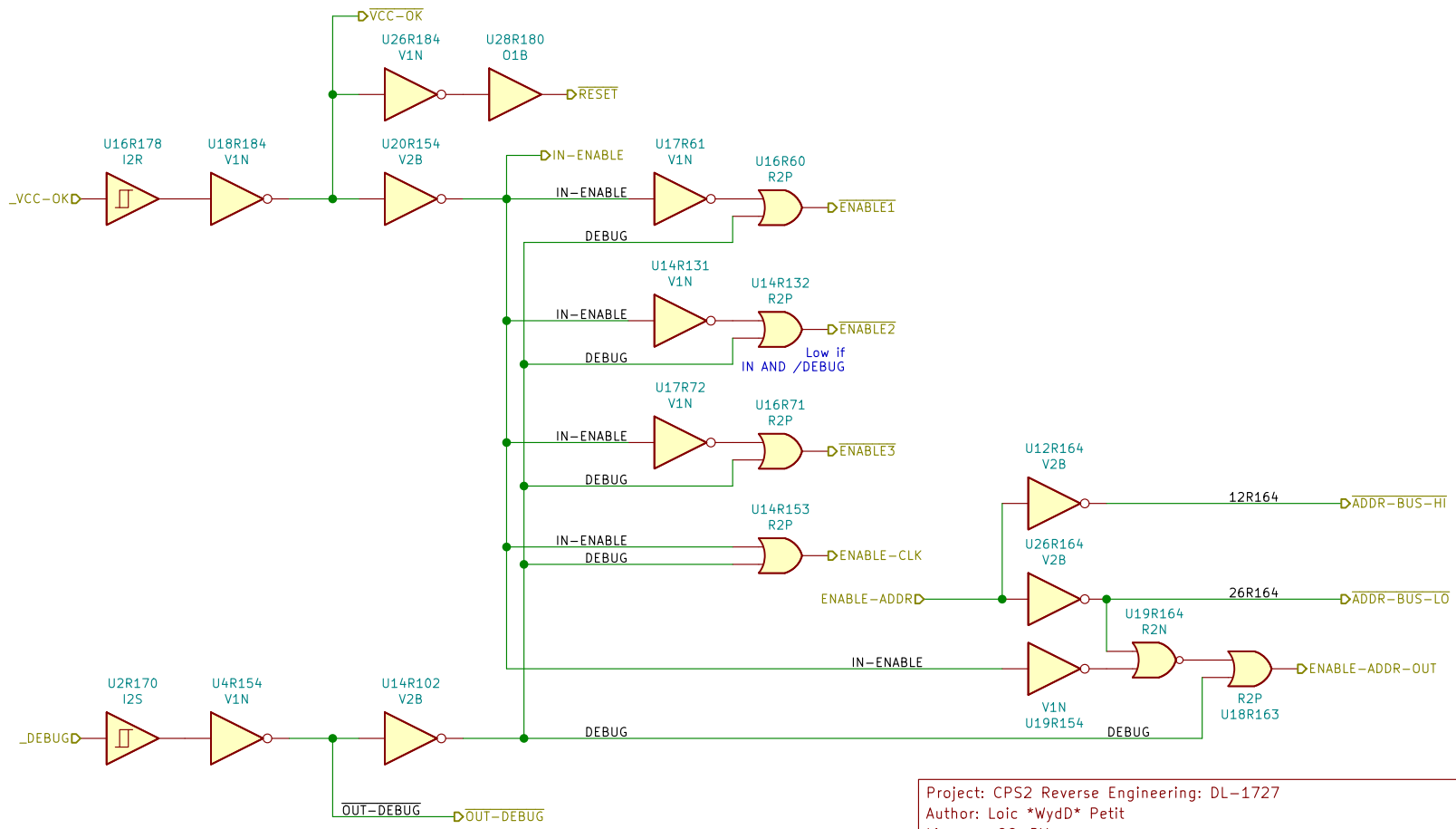
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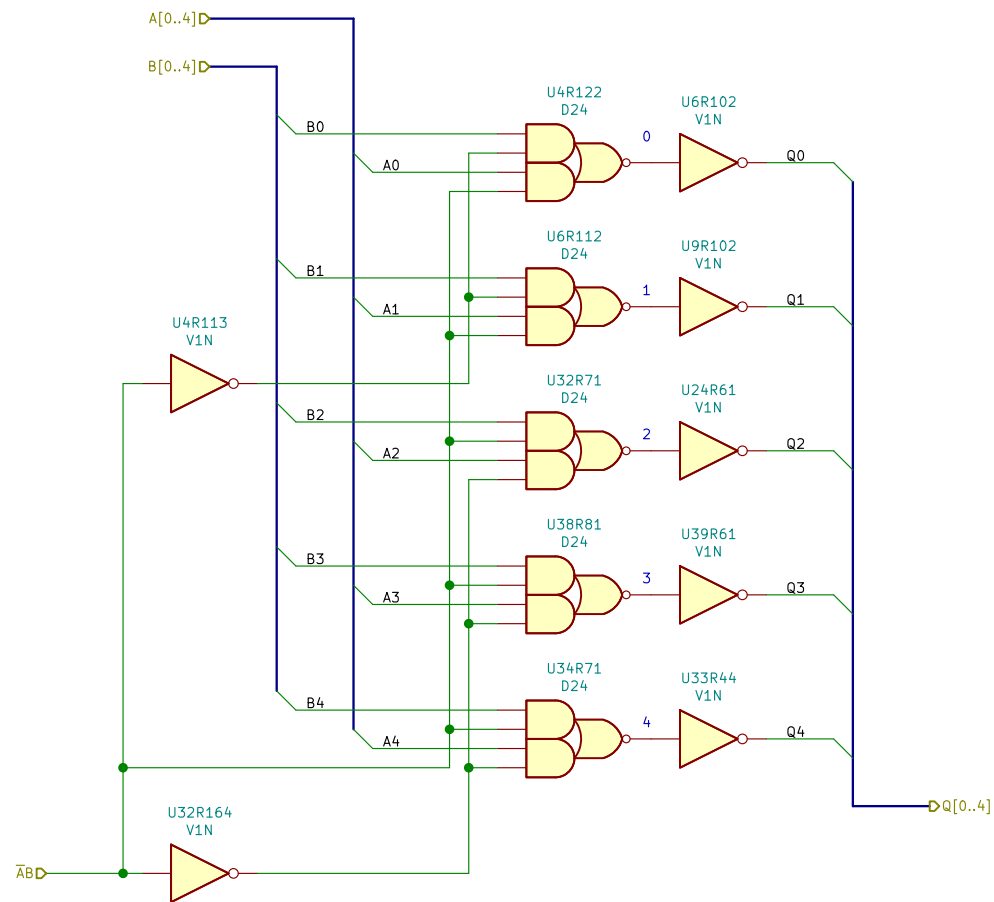
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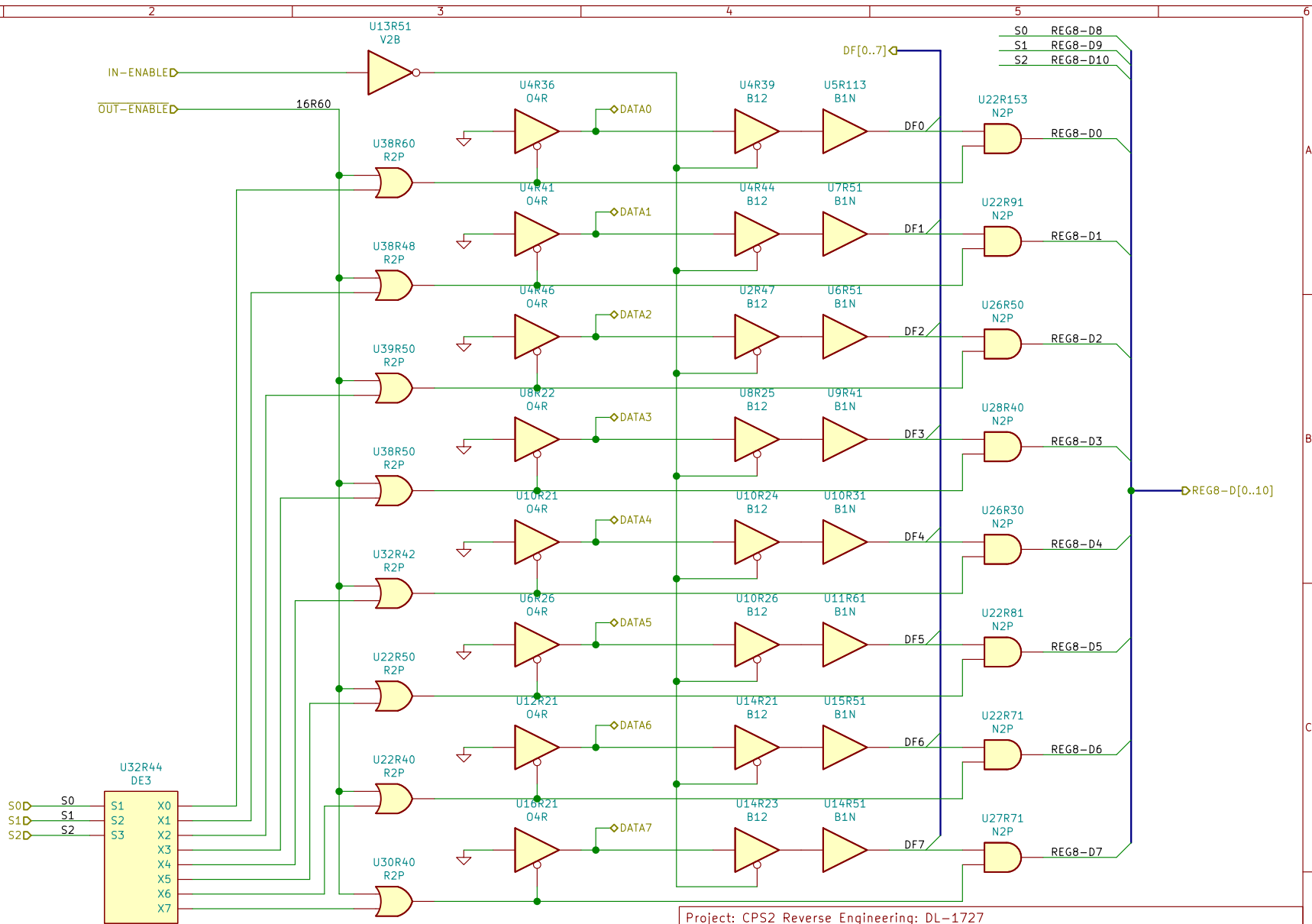
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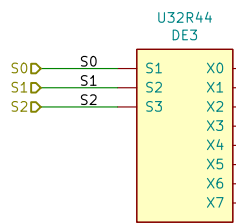
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S0 REG8-D8
 S1 REG8-D9
 S2 REG8-D10



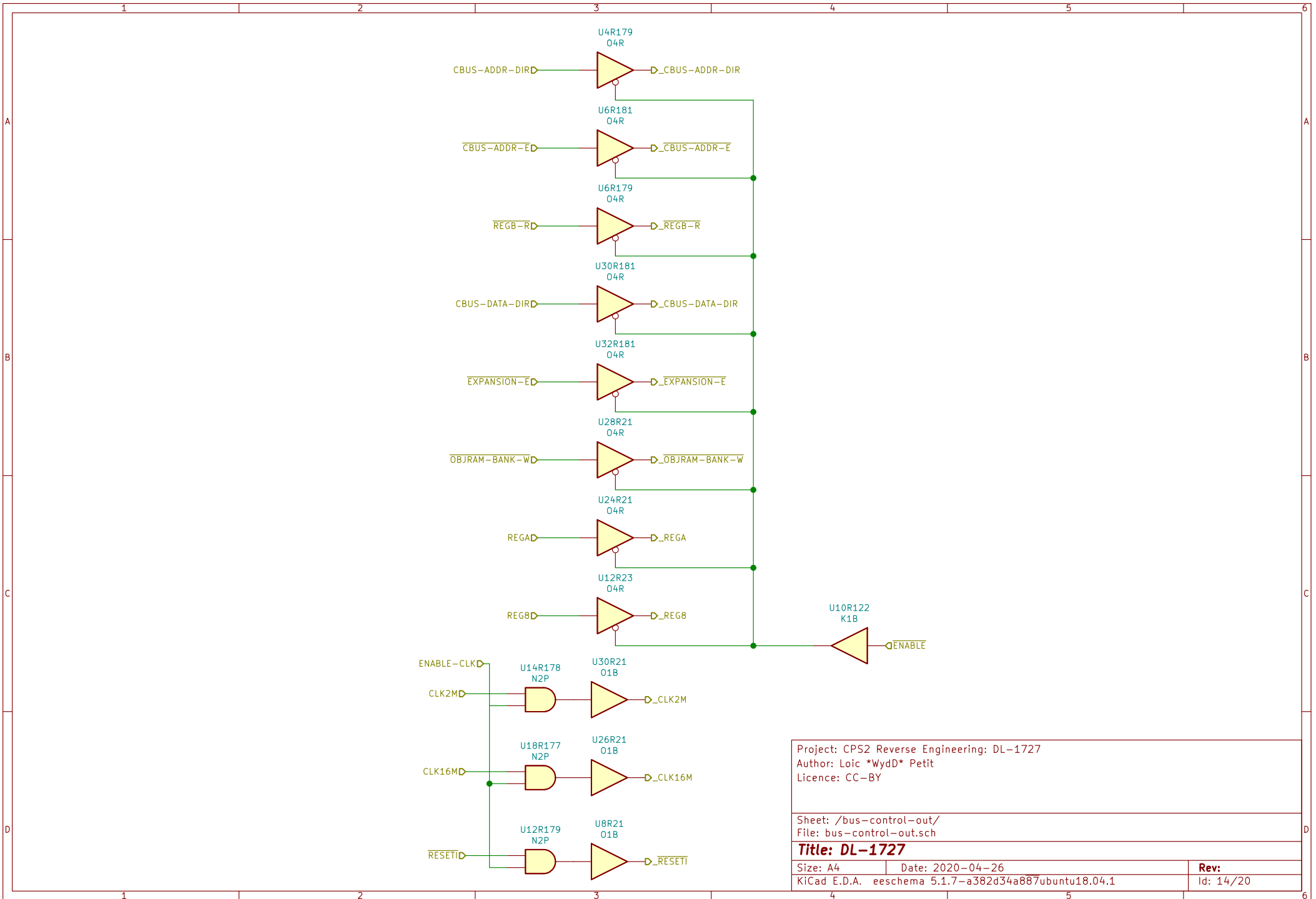
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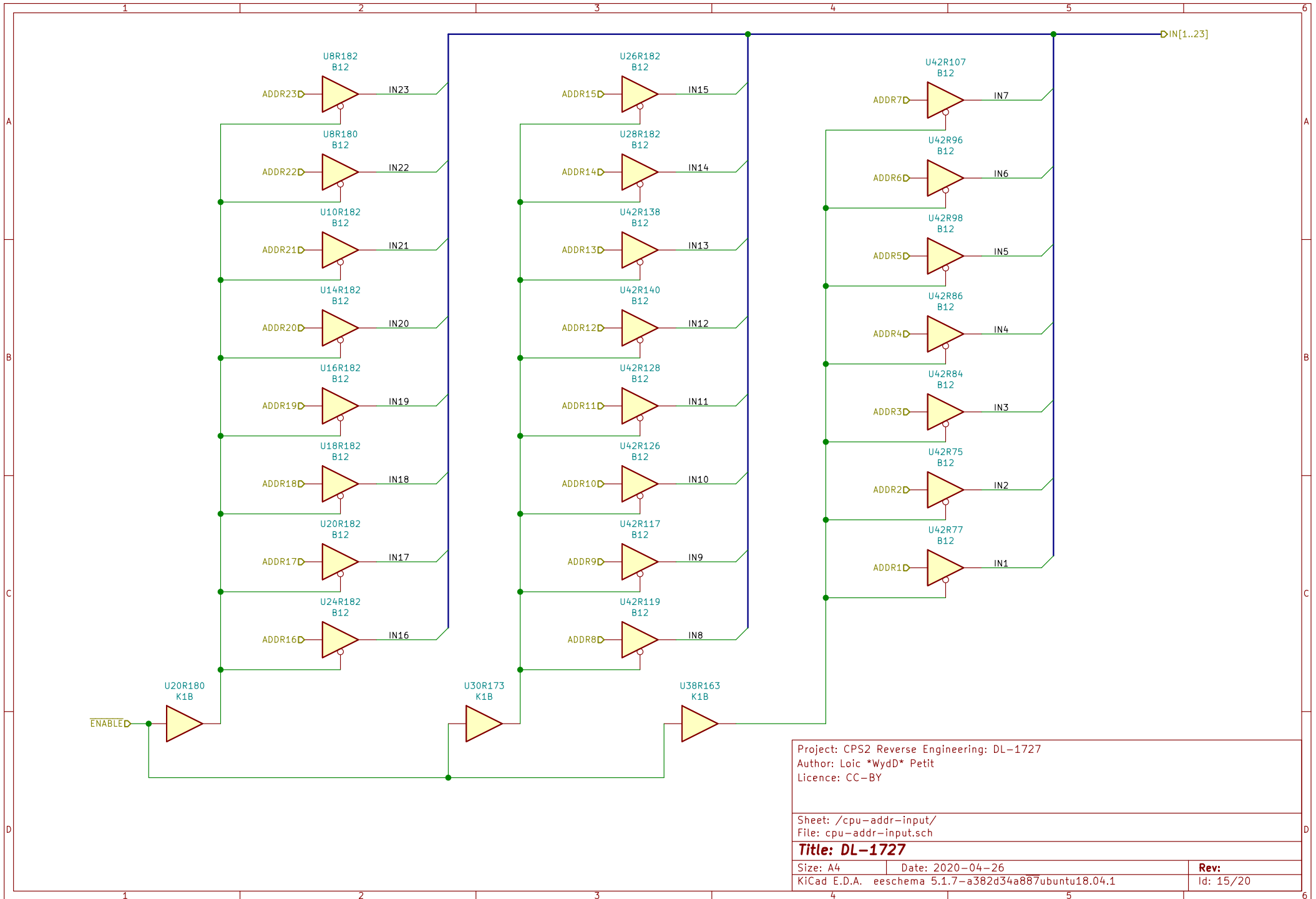
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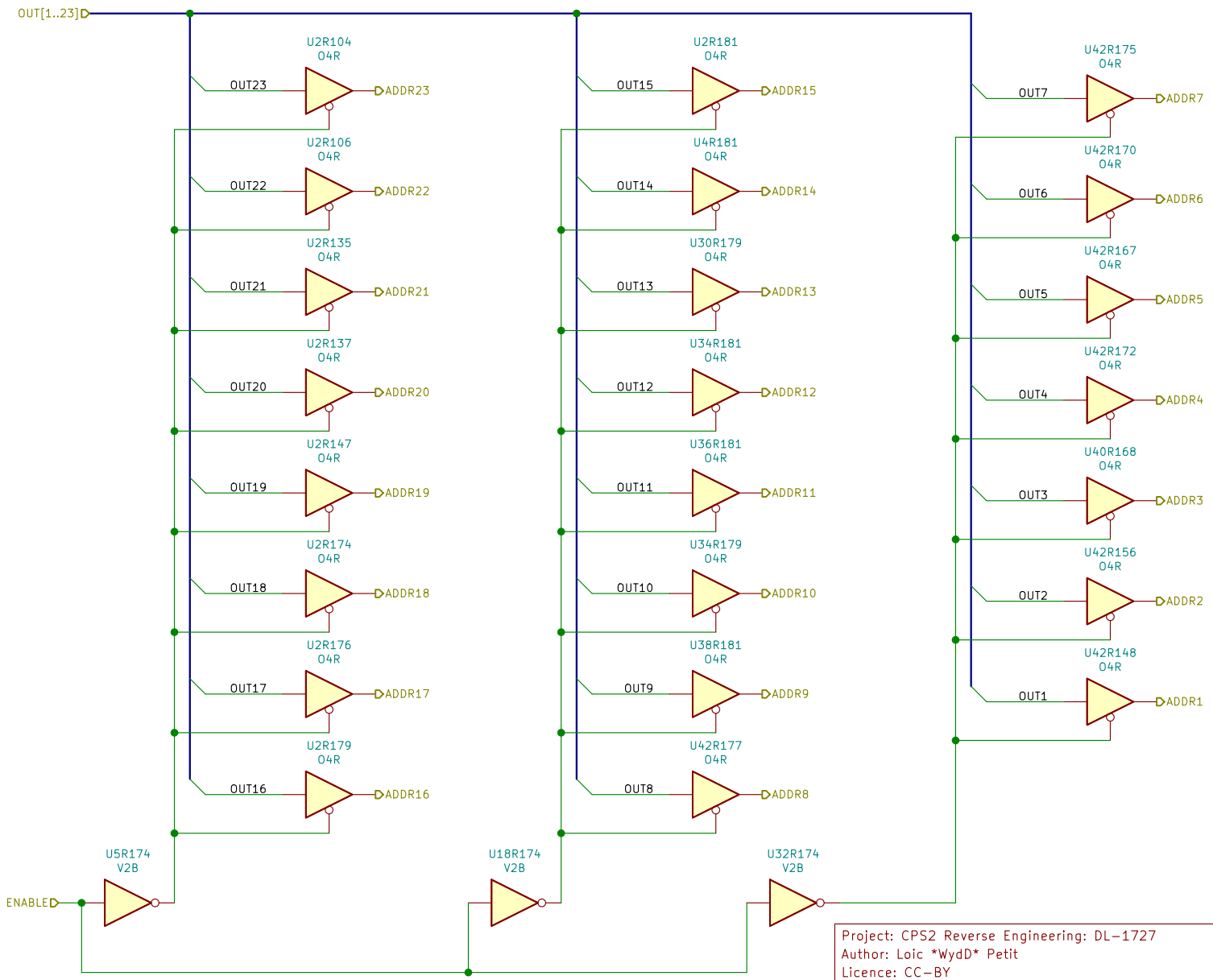
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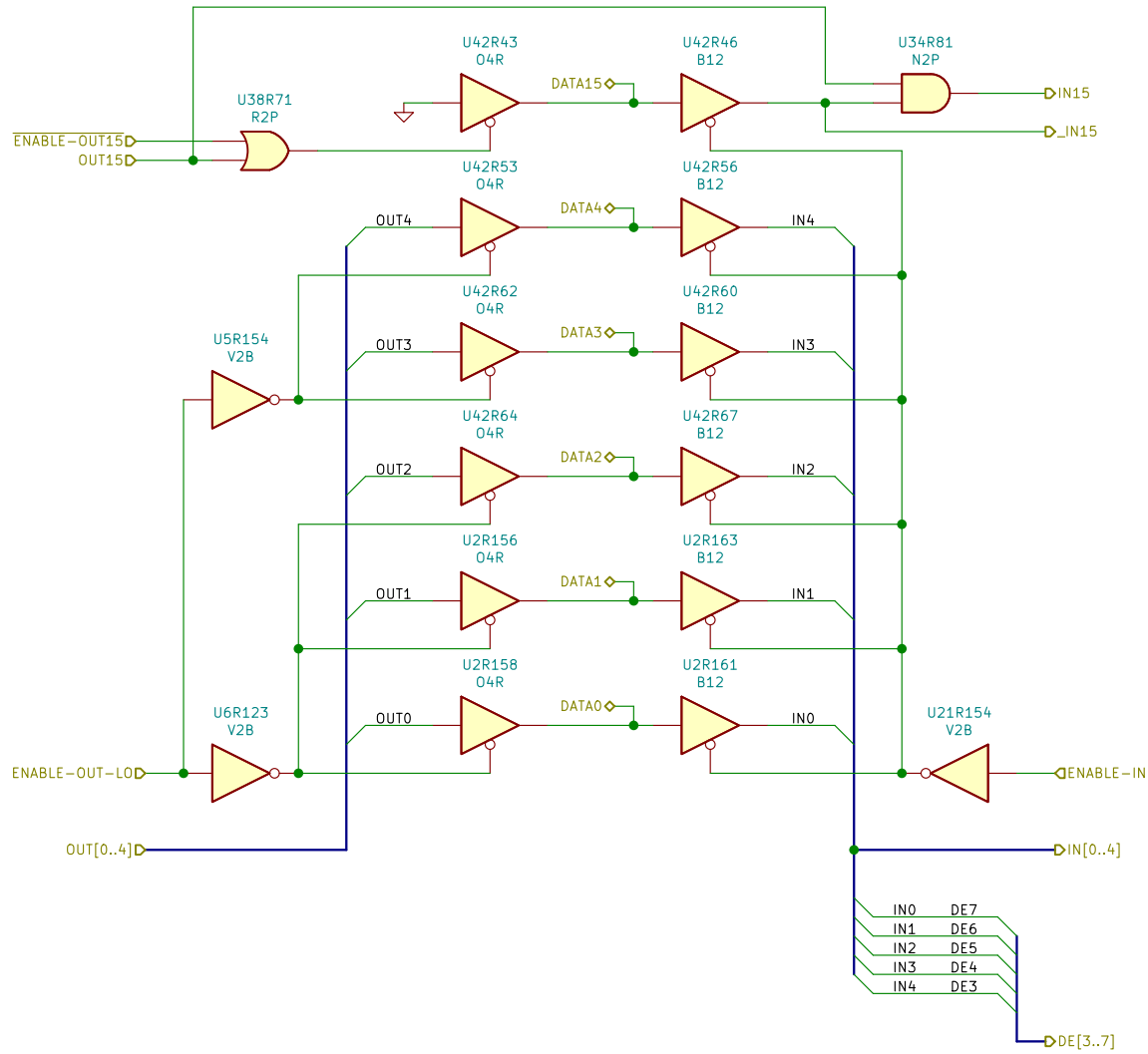
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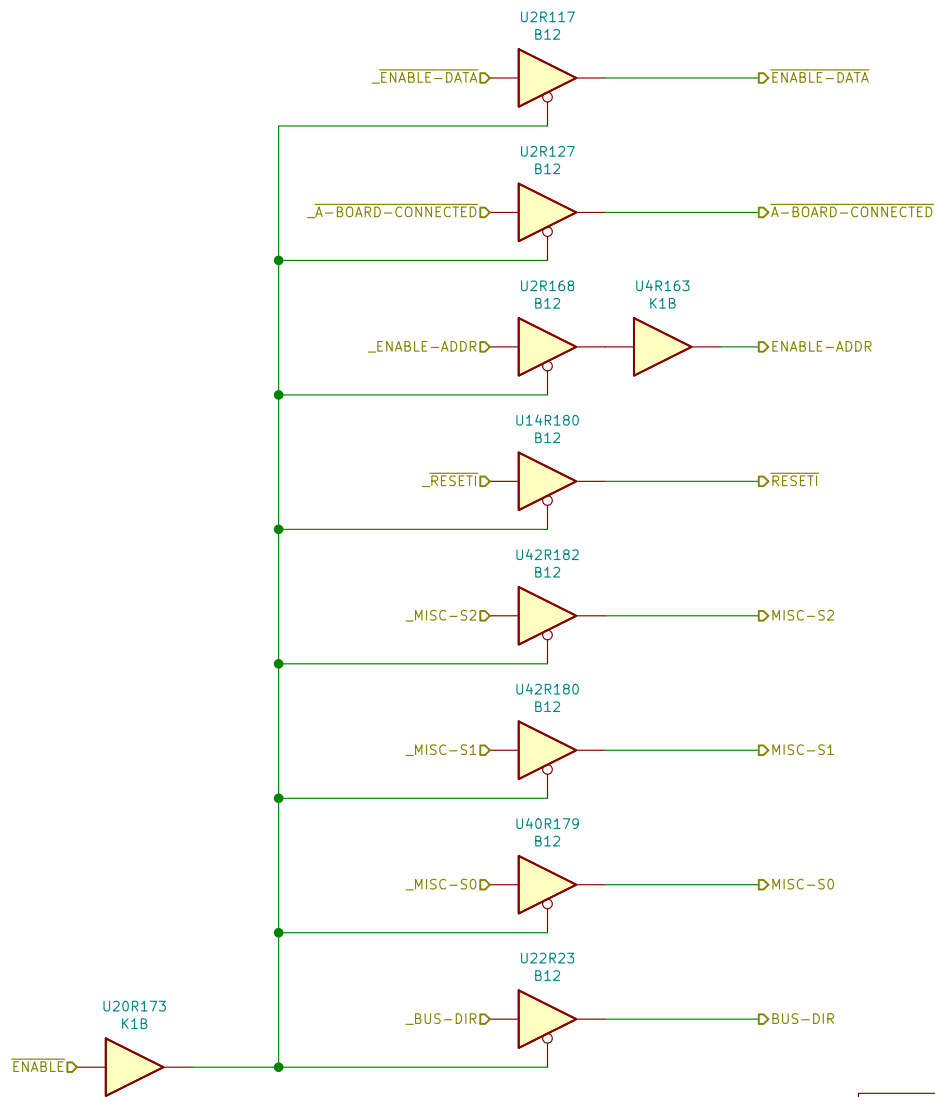
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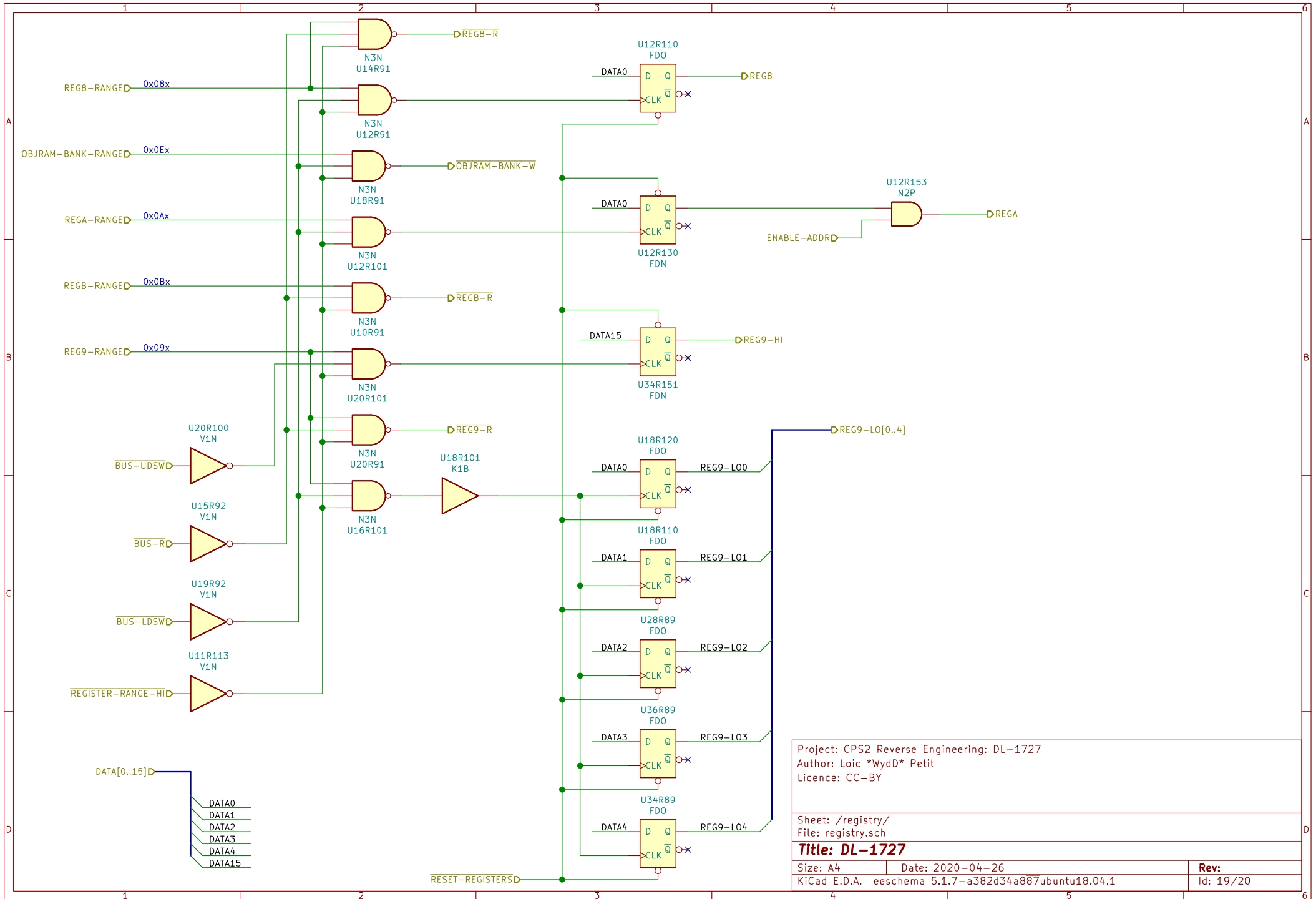
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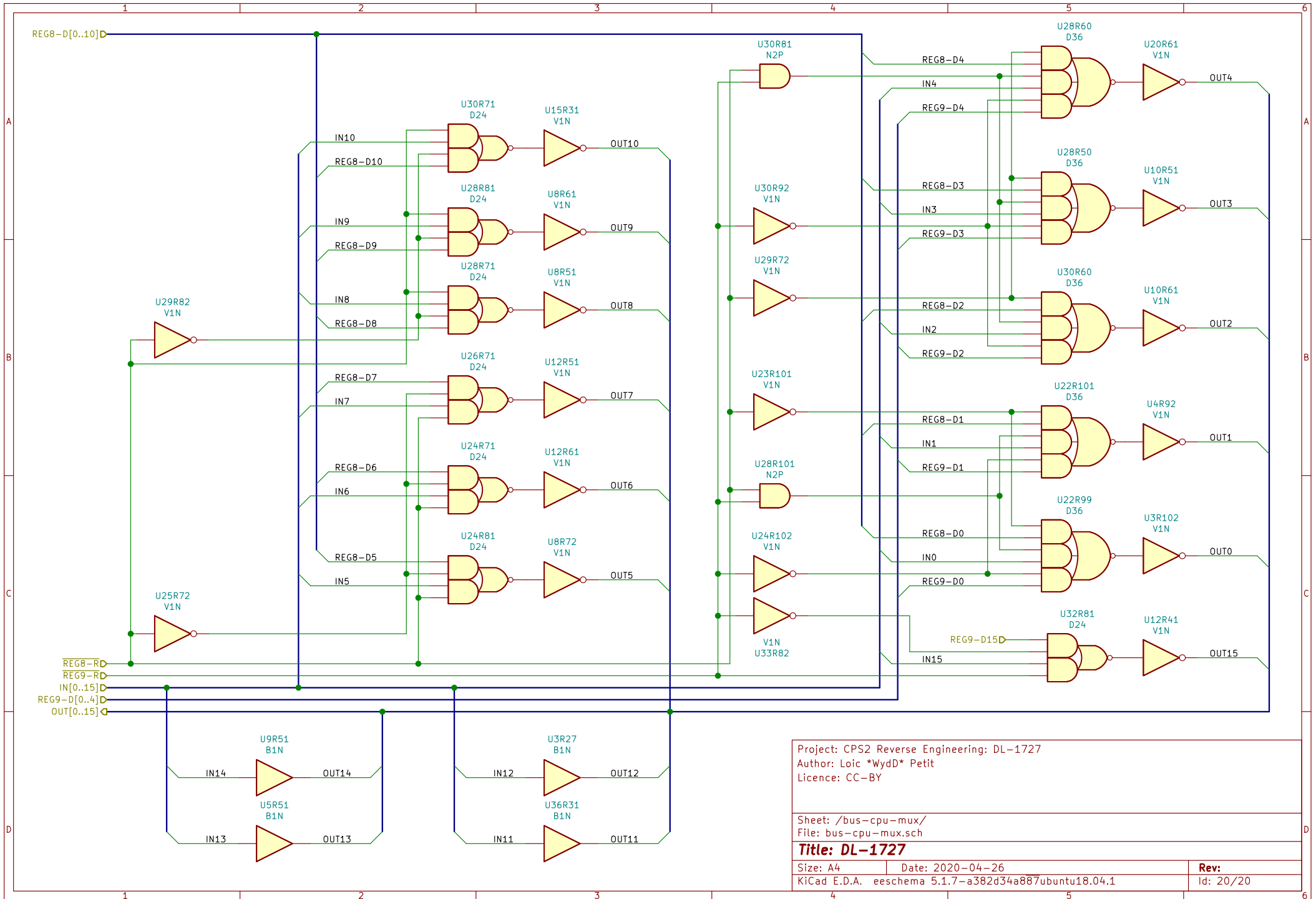
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