MAIN CPU BUS

CA[1..23]

CD[0..15]

VIDEO TIMINGS

From the video counter, this will generate the main graphics timings. And the main sprite reset timing.

It also takes care of the default 'ROMA[20..22]' values (unless WSTROM is in use)

Sheet: video-timings

File: video-timings.sch

VIDEO COUNTER

Sheet: video-counter

DEBUG1 stops the counter increment
DEBUG4 resets the counter to the init value

Produces the LINE / COL bus mainly using the CLK4M pulse.

You can change the initialization values using the SCANLINE register.

Very similar to the CPS-B counter. But it has a HSYNC/VSYNC as input. It is surely there to synchronize two boards together.

File: video-counter.sch

Sheet: main-signals

File: main-signals.sch

Sheet: addr-decoder

All signals here are write on the main BUS with the hardwired addresses.

File: addr-decoder.sch

Sheet: bus-data-io

File: bus-data-io.sch

CPS-ID

Sheet: cps-id

Only readable register of the A-01.

Provides an ID similar to CPS-B-21. But the ID is hardwired to 0. It still contains a read counter which could be used for security.

File: cps-id.sch

CA can set as output using the bus request. It is driven as the ADDR bus.

WSTROM

The WSTROM phase is not used in the final release.
The idea is to write a 64k page from RAM to video data.
The PLxWED are flags to write on specific chips.
The CPS-B-21 will transmit data to the chips.
The BUS-REQUEST becomes available after a write on WSTROM-COPY

Sheet: wstrom

File: wstrom.sch

WSTLUT

During the WSTLUT phase, The ADDR bus iterates on the RAM addresses where the palette is. The CPS-B will take care of pointing the palette ram to the right address and do the write.
The BUS-REQUEST happens after a write on PALETTE-BASE

Sheet: wstlut

File: wstlut.sch

MAIN BUS

BUS REQUEST SIGNALS

BUS REQUESTS MODULE

This module synchronizes all the bus requests intents that the A-01 needs to perform. Once a bus request is decided BR goes low. When BGACK goes low, BUS-READY becomes high. ADDR becomes usable and the correct BUS-*** signal becomes low.

The end of the bus request is given by a specific signal (***-END).

Sheet: bus-requests

File: bus-requests.sch

During bus requests for scrolls operations, this module sets the address of the ram to get the scroll data back.
This data is then put inside the SRAM.

SCROLL BUS ADDRESS

Sheet: scroll-bus-addr

File: scroll-bus-addr.sch

Sheet: scroll-positions

File: scroll-positions.sch

SCROLL POSITIONS

During graphics raster, this module will compute the correct X/Y coordinates. The stars doesnt require the SRAM so it will directly outputs to the GFX bus.

REGISTER SIGNALS

XS[0..4]

The SRAM acts as a buffer that stores the scroll data for the current row of all scroll layers.
It contains 256 entries of 16+10 bits.

It is written during the bus requests and it is read during the raster.

SCROLL SRAM

Sheet: scroll-sram

File: scroll-sram.sch

GFX TIMINGS

GFX DATA BUS

This module takes the graphics bus and converts it to GFX ROM addresses and data sent to the CPS-B for raster.

It can be interpreted as a big multiplexer which will provide the correct output based on the commun bus data and on each layer.

ROMA-OUT

Sheet: raster-out

File: raster-out.sch

Sheet: roma-bus

File: roma-bus.sch

Sheet: sram-debug

Outputs internal data to ROMA / CB for testing purposes

DEBUG3 outputs the current RAM data
RAM address is set by CA and WR

DEBUG2 outputs the video counter

File: sram-debug.sch

SPRITES

The sprite controller reads the sprite entries from the main BUS and assembles the data to the graphics bus.

Only the ADDR and flip attributes are used by the ROMA controller. The CB bus is used by the VRAM controller.

Sheet: sprites-controller

It's important to note that the graphics bus is not used as a raster because it happens during HBLANK. It is only there to send the colour data via the CPS-B to the VRAM.

File: sprites-controller.sch

VRAM

The VRAM stores the sprites data in double buffer. During one frame, one side is reading, the other side is writting new data.

During read operations:
- The address of the sprite to draw is written in XA[0..7] based on the video counter.
- The data is fed by the VRAM to the CPS-B.

During write operations:
- The address of the sprite is written in XA[0..7] based on the X/Y attribute of the sprite.
- The data is mainly the CB part of the gfx bus (the palette id) which is fed by the sprites controller. The 4 LSB are provided directly by the CPS-B

The VRAM is a CAS/RAS-based serial RAM which makes the logic a bit hard to follow.

Sheet: vram-controller

REWEN is given by the CPS-B.
Tells if we should write the data or not (= if colour is transparent)

File: vram-controller.sch

CB[0..5]

XSEL

CDEN

CPC[0..1]

ROMA[0..22]

AA[0..7]

ACAS[0..1]

ASOE[0..1]

ASCK

ADTOE

AD[4..12]

BA[0..7]

BCAS[0..1]

BSOE[0..1]

BSCK

BDTOE

BD[4..12]

Author: Loïc "WydD" Petit
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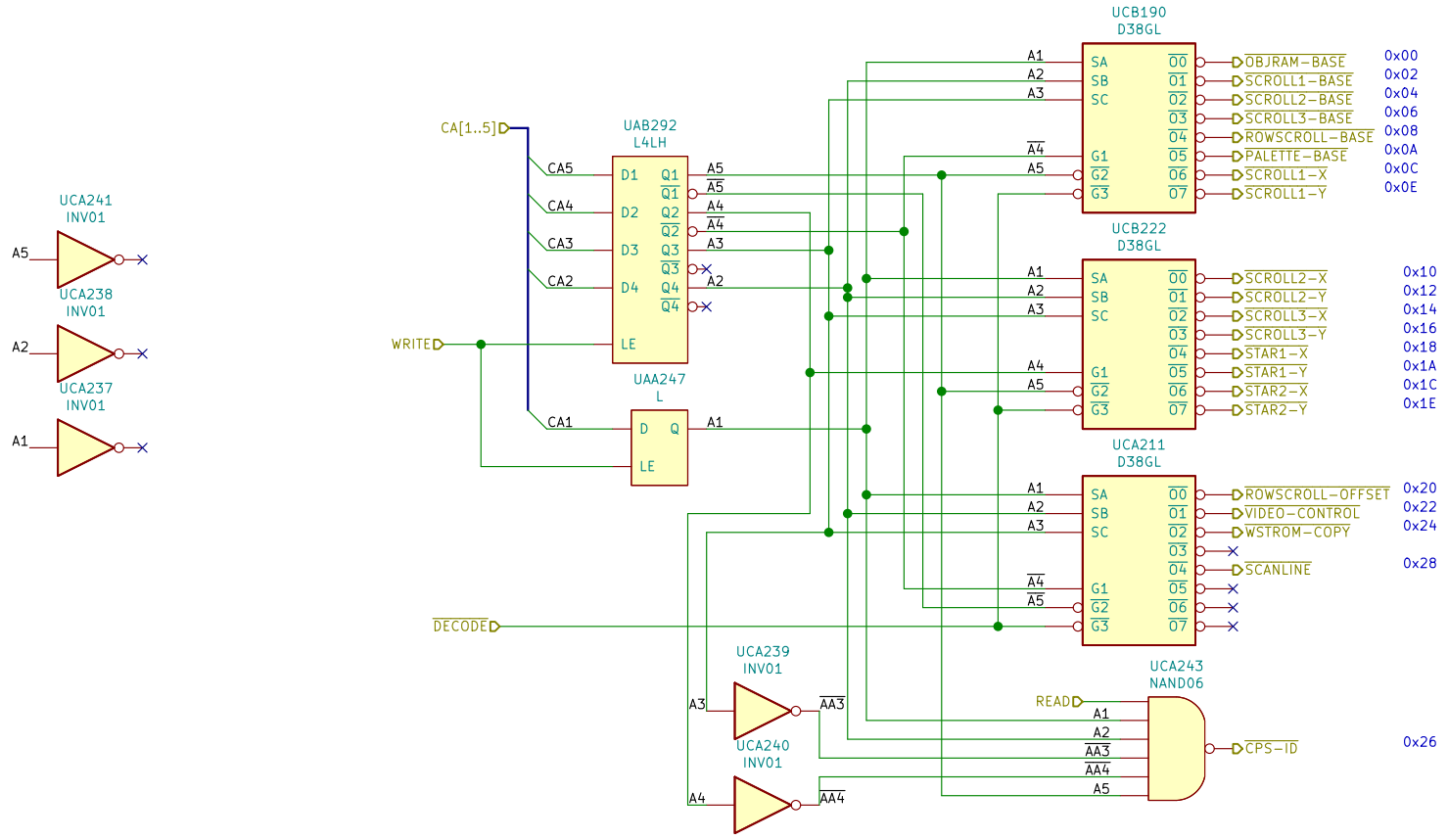
Sheet: /
File: DL-0311.sch

Title: CPS Reverse Engineering: DL-0311

Size: A2	Date: 2021-09-12	Rev:
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 1/83

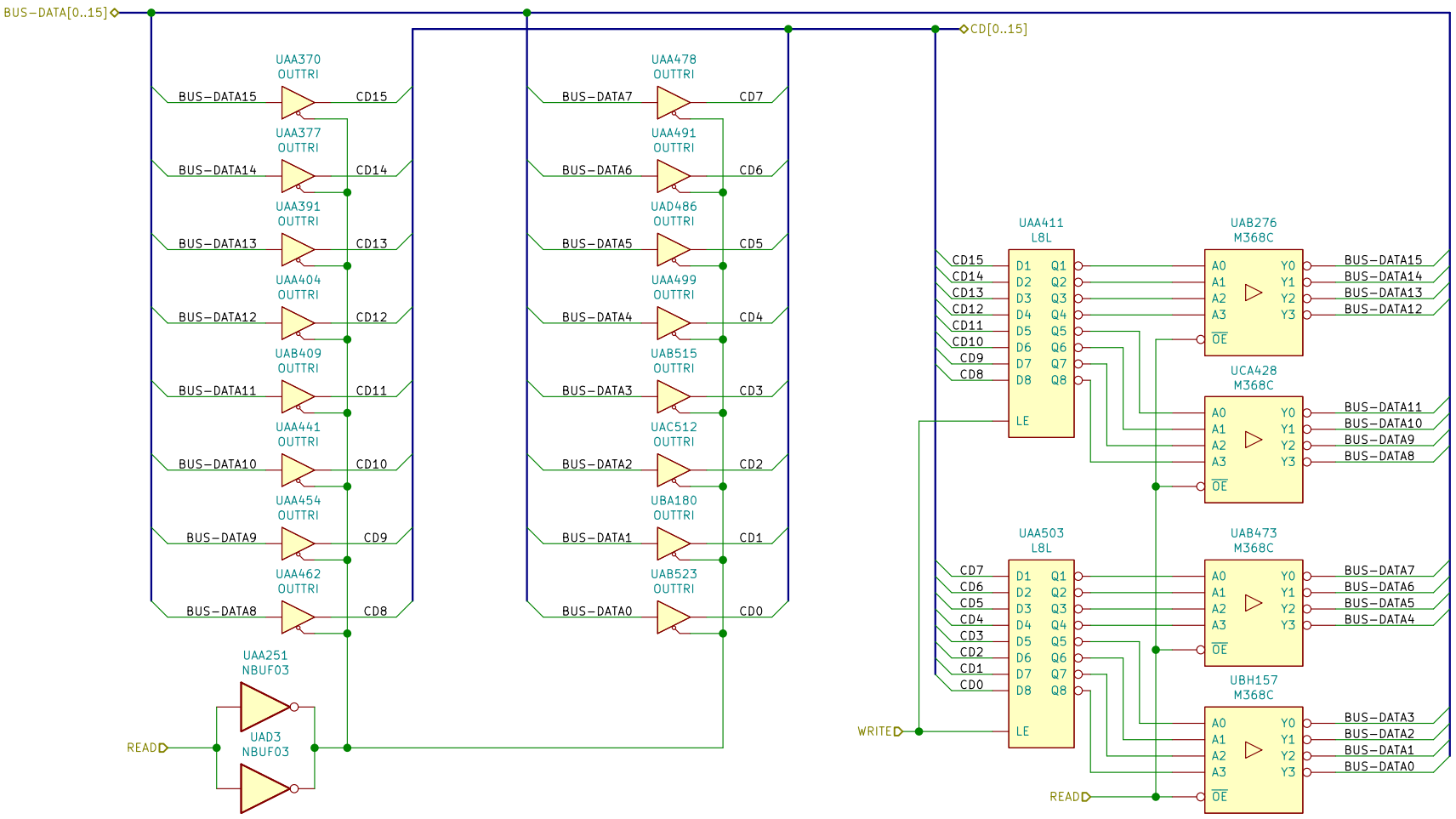


Author: Loïc *WydD* Petit
Licence: CC-BY

Sheet: /addr-decoder/
File: addr-decoder.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 2/83



Author: Loïc *WydD* Petit
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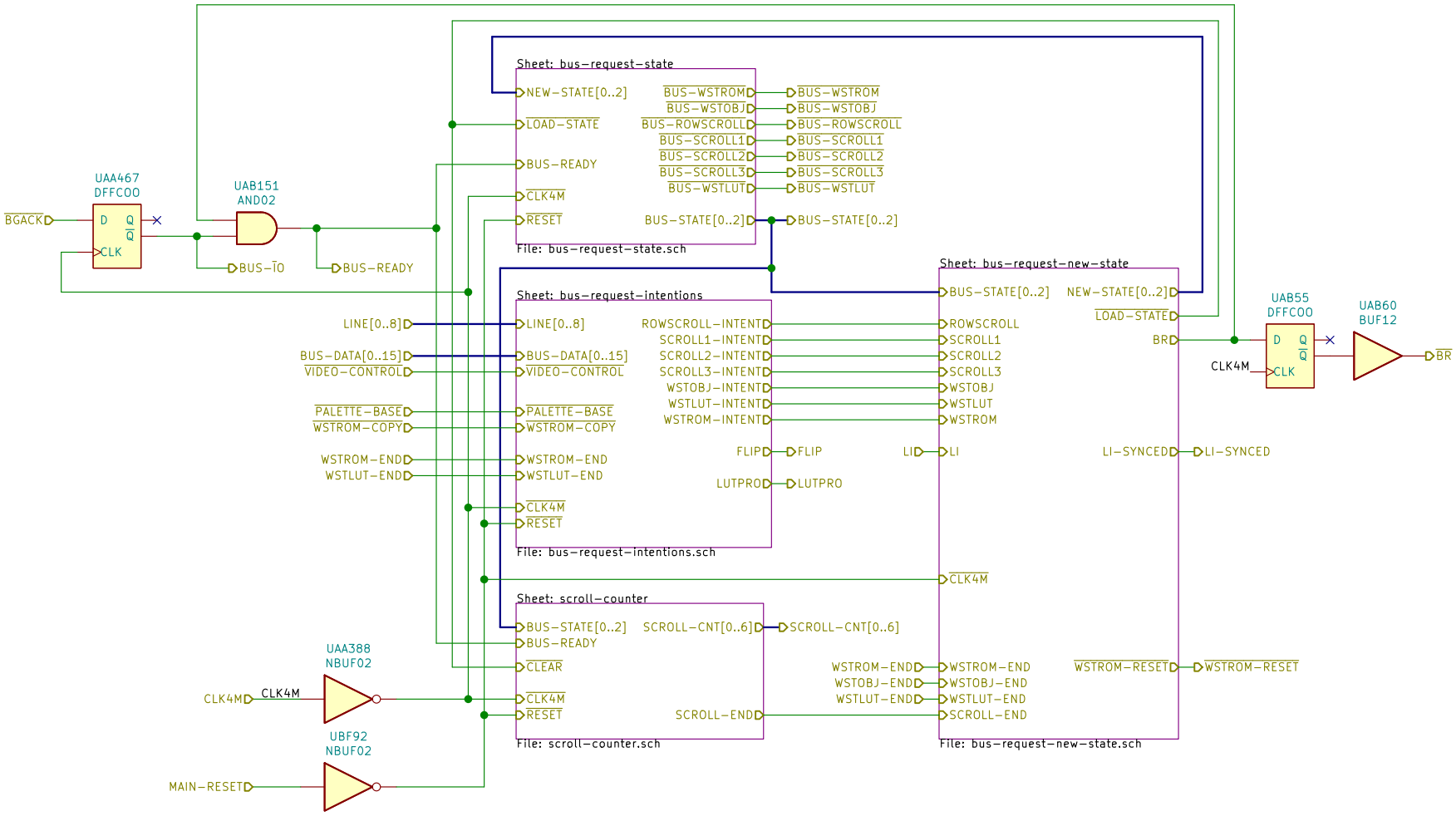
Sheet: /bus-data-io/
File: bus-data-io.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 3/83



The implementation is a complex state machine.
The state a 3 bit value, each value correspond to a specific bus request.

The intentions are defined by either a LINE value or a write on some registers.
Then the state transition will take the 3 bit value and produce a new state
after line increment.

Report to the extra documentation to see the state machine in action.

Author: Loïc *WydD* Petit
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Sheet: /bus-requests/
File: bus-requests.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 4/83

UBE0
NAND06
LINE0
LINE1
LINE2
LINE3
LINE7
LINE8
UBD13
NAND03
LINE4
LINE7
LINE8
UBD3
NAND03
LINE5
LINE7
LINE8
UBC14
NAND03
LINE6
LINE7
LINE8
UBD22
NAND03
LINE6
LINE7
LINE8
UBD35
NAND03
LINE5
LINE7
LINE8
UBD10
NAND04
LINE2
LINE4
LINE7
LINE8
UBD0
NAND04
LINE1
LINE4
LINE7
LINE8
UBD7
NAND04
LINE0
LINE4
LINE7
LINE8
UBE24
NAND04
LINE3
LINE4
LINE7
LINE8
UBD15
NAND13
VCC
$\overline{6}$ & (
0 & $\overline{1}$ & 2 & 3 & $\overline{7}$ & $\overline{8}$
4 & $\overline{7}$
5 & $\overline{7}$
$\overline{6}$ & $\overline{7}$
$\overline{6}$ & 7
$\overline{5}$ & $\overline{7}$
$\overline{4}$ & $\overline{3}$ & 7
$\overline{4}$ & $\overline{2}$ & 7
$\overline{4}$ & $\overline{1}$ & 7
$\overline{4}$ & 0 & 7
)
00xxx1111
001xxxxxx
00x1xxxxx
00xx1xxxx
010xxxxxx
01x0xxxxx
01xx00xxx
01xx0x0xx
01xx0xx0x
01xx0xxx0
UBD38
AND02
VC0
ROWSCROLL-INTENT
15 <= x < 240
UBB48
NAND06
LINE0
LINE1
LINE2
LINE3
LINE6
LINE8
UBB34
NAND06
LINE0
LINE1
LINE2
LINE3
LINE5
LINE8
UBB42
NAND06
LINE0
LINE1
LINE2
LINE3
LINE7
LINE8
UBB40
NAND04
VC2
UBB24
AND02
SCROLL2-INTENT
x mod 16 AND x < 240
UBB26
NAND06
LINE0
LINE1
LINE2
LINE3
LINE4
LINE8
UCA163
NAND13
LINE0
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
VCC
510 (aka -2)
UBB5
NAND02
VC3
UBB6
AND02
SCROLL3-INTENT
x mod 32 AND x < 240
OR x == -2
BUS-DATA[0..15]
UBE29
M175C
BUS-DATA3
BUS-DATA2
BUS-DATA1
BUS-DATA0
D0
D1
D2
D3
Q0
Q1
Q2
Q3
CLK
R
VC3
VC2
VC1
VC0
UAD190
BUF12
UBF24
DFFCOR
D
Q
CLK
BUS-DATA15
VC15
UAD222
BUF12
FLIP
UBH32
OR02
VIDEO-CONTROL
CLK4M
RESET
UBE71
DFFCOR
WSTROM-INTENT
CLK4M
RESET
UBE68
OAI21
WSTROM-END
WSTROM-COPY
UBE106
DFFCOR
LUTPRO
CLK4M
RESET
UBF89
OAI21
WSTLUT-END
PALETTE-BASE
Default state:
-> LUTPRO = 0
If someone writes in PALETTE-BASE
-> LUTPRO = 1
Wait until WSTLUT-END = 1
-> LUTPRO = 0 back to default
LINE[0..8]
UBD52
NBUF02
UAD331
NBUF02
UBG3
NBUF02
UBG71
NBUF02
UBA16
NBUF02
UBC18
NBUF02
UBA49
NBUF02
UAD257
NBUF02
UAB252
NBUF02
LINE0
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
UAD335
NAND06
UAC316
NAND06
UAC304
NAND06
UAD316
NAND06
UBB16
NAND06
UBC8
NAND06
UBA3
NAND06
$\overline{0}$ & $\overline{1}$ & $\overline{2}$ & $\overline{8}$ & OR(
3 & $\overline{7}$
4 & $\overline{7}$
5 & $\overline{7}$
6 & $\overline{7}$
7 & $\overline{4}$
7 & $\overline{5}$
7 & $\overline{6}$
)
UAD296
NAND08
VCC
UAD276
AND02
VC1
SCROLL1-INTENT
1 if x mod 8 AND 8 <= x < 248
UBC43
NAND04
UBC49
NAND04
UBC52
NAND03
LUTPRO
VBLANK
UBA52
AND02
WSTLUT-INTENT
VBLANK.LUTPRO
x < 16 OR
x >= 240 OR
x >= 256
UBA19
NAND08
240-243
UBE8
NAND13
239
VCC
UBD25
AND03
WSTOBJ-INTENT
Everything unless 239-244
UBD30
NAND08
240
244

Author: Loïc *WydD* Petit
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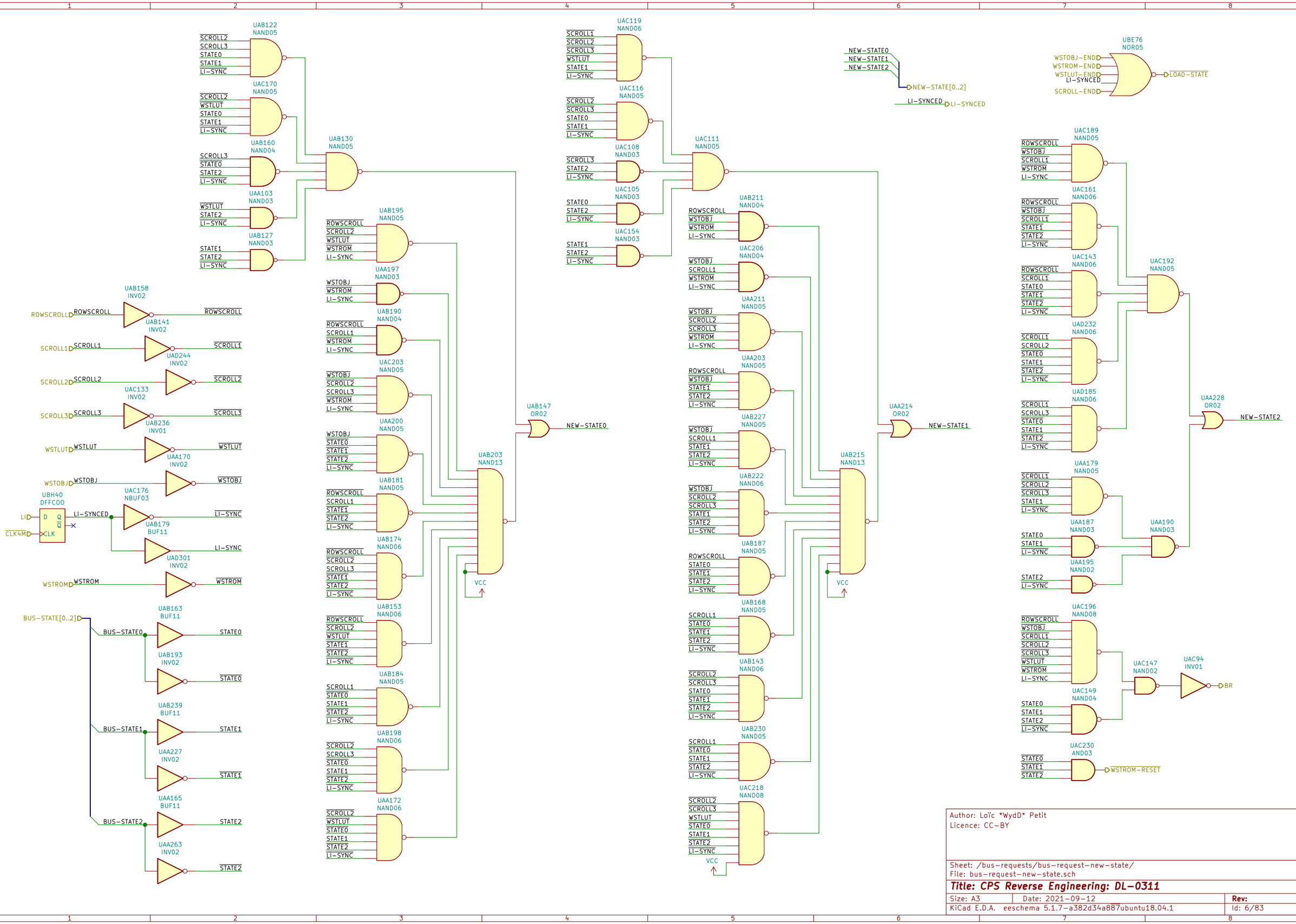
Sheet: /bus-requests/bus-request-intentions/
File: bus-request-intentions.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 5/83



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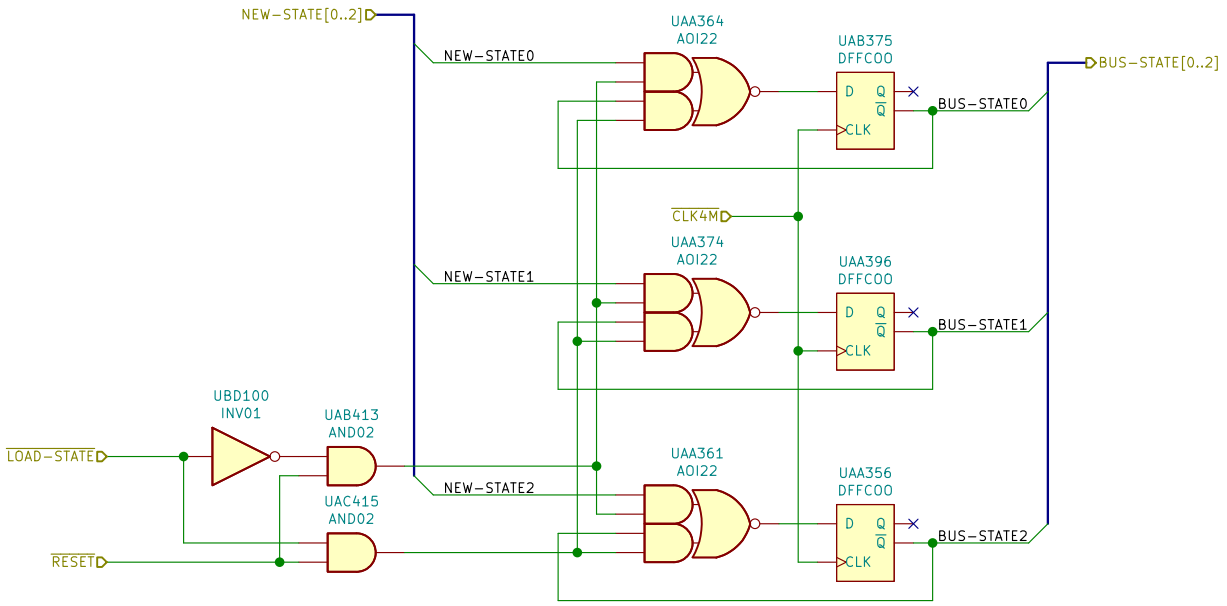
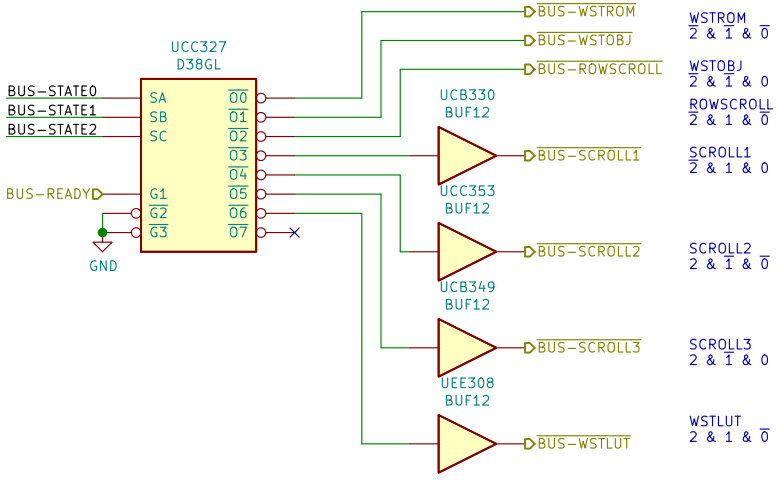
Sheet: /bus-requests/bus-request-new-state/
File: bus-request-new-state.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 6/83	





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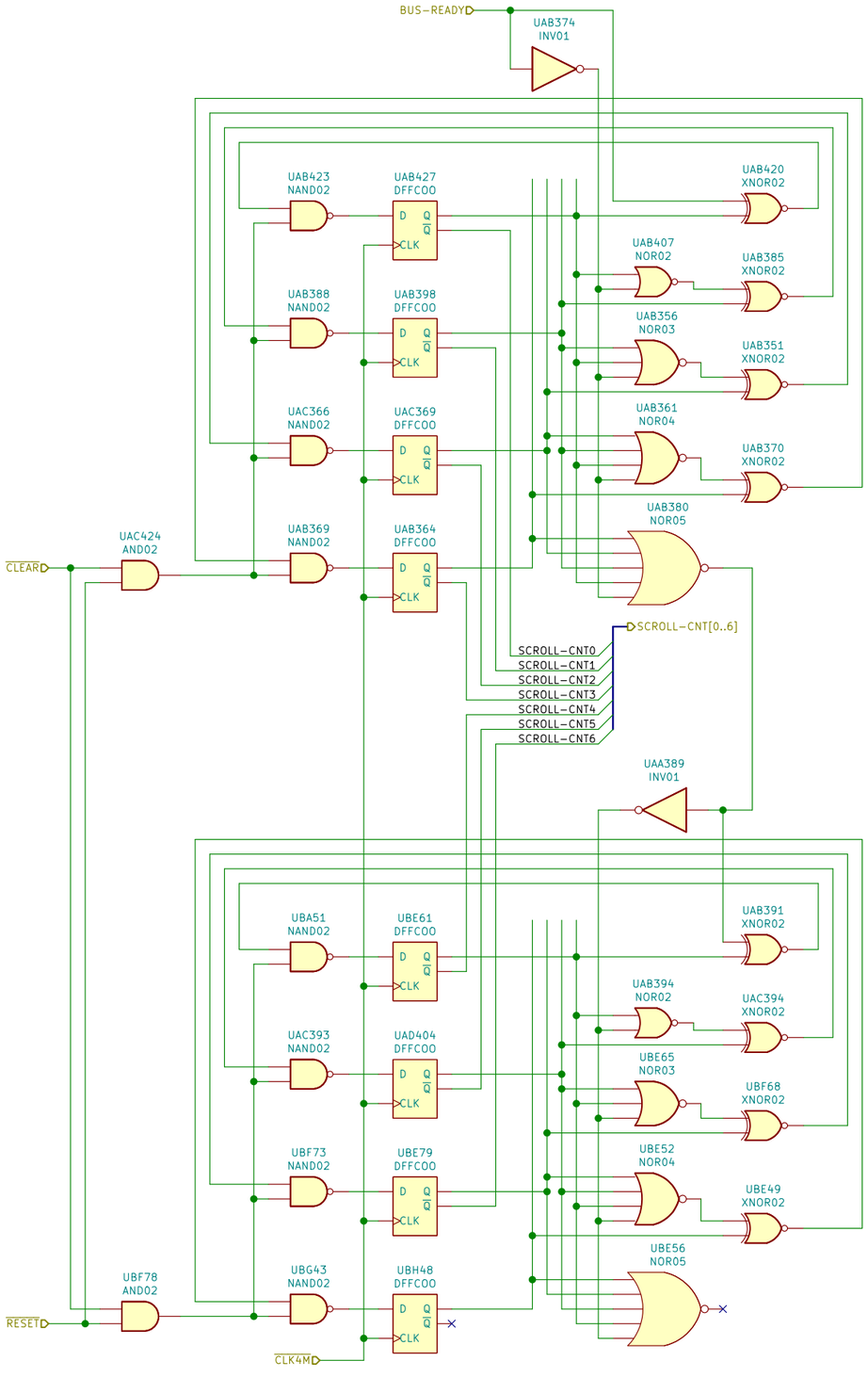
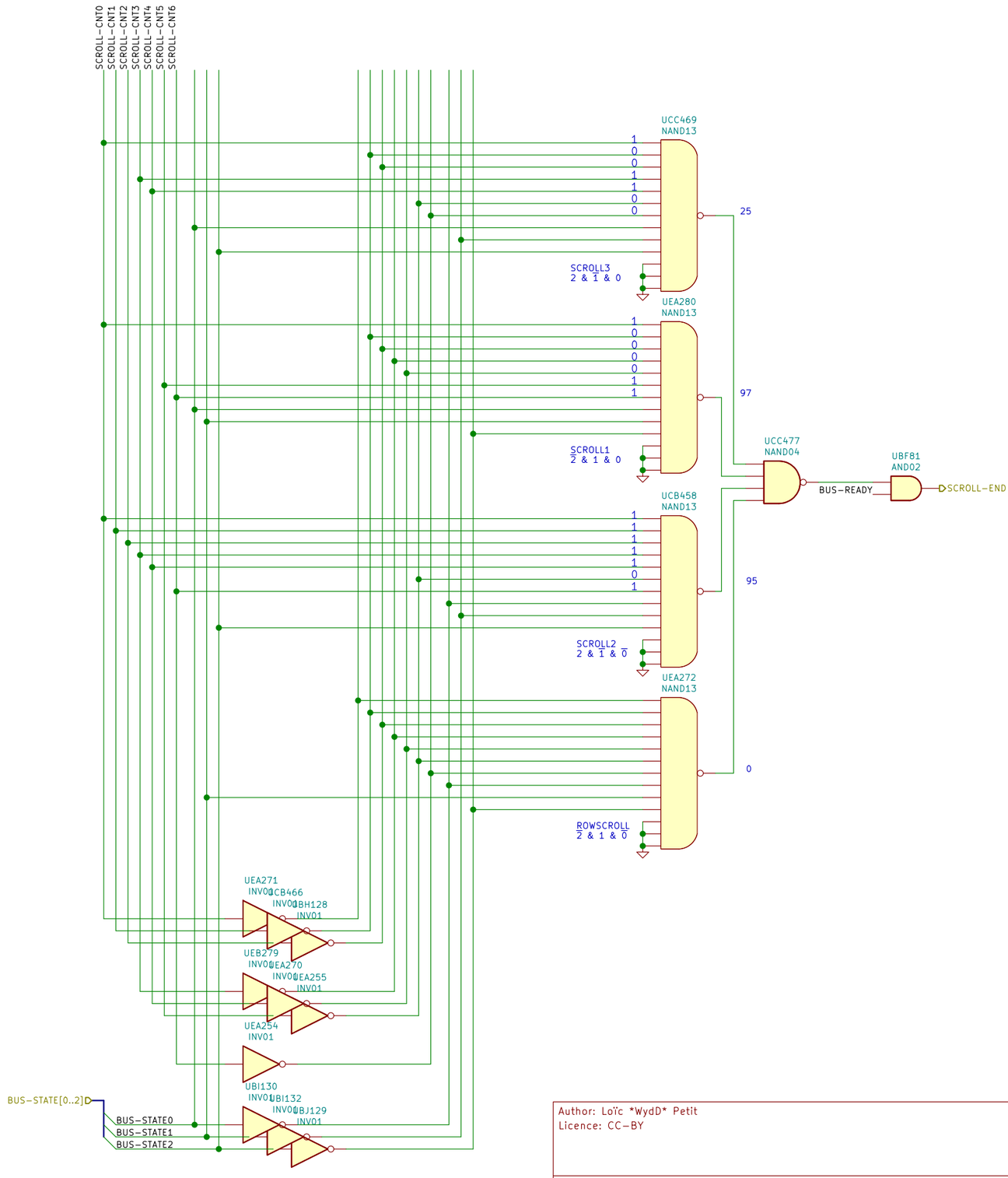
Sheet: /bus-requests/bus-request-state/
File: bus-request-state.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 7/83





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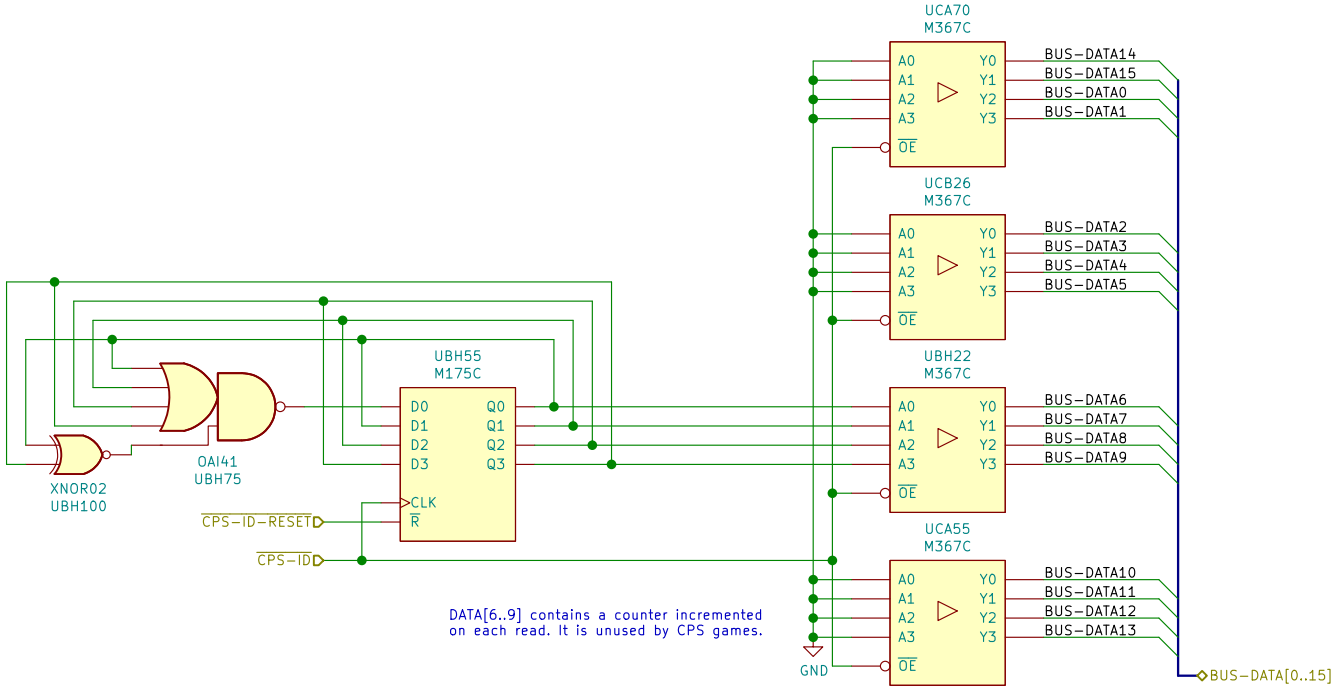
Sheet: /bus-requests/scroll-counter/
File: scroll-counter.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 8/83



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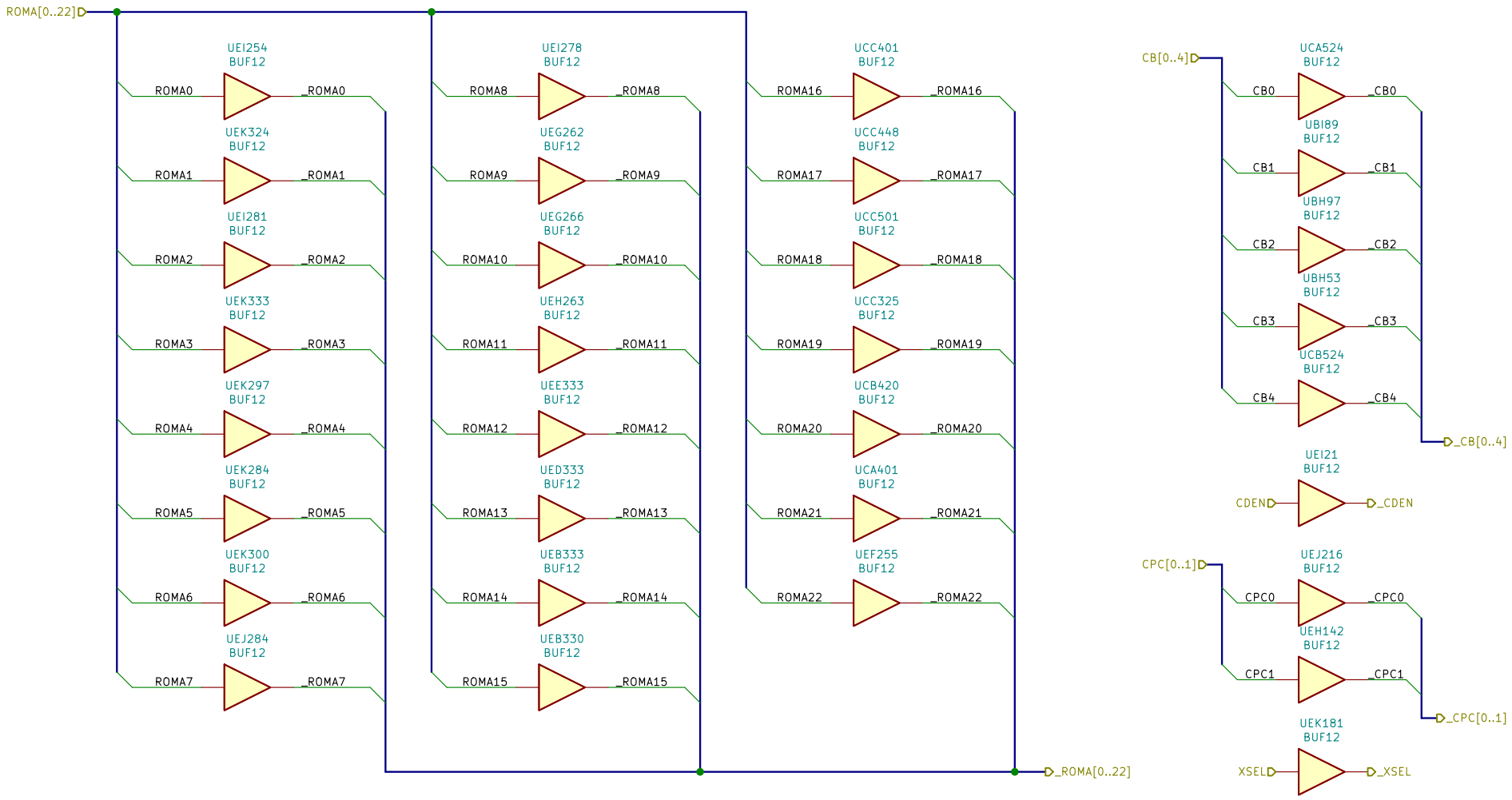
Sheet: /cps-id/
File: cps-id.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 9/83



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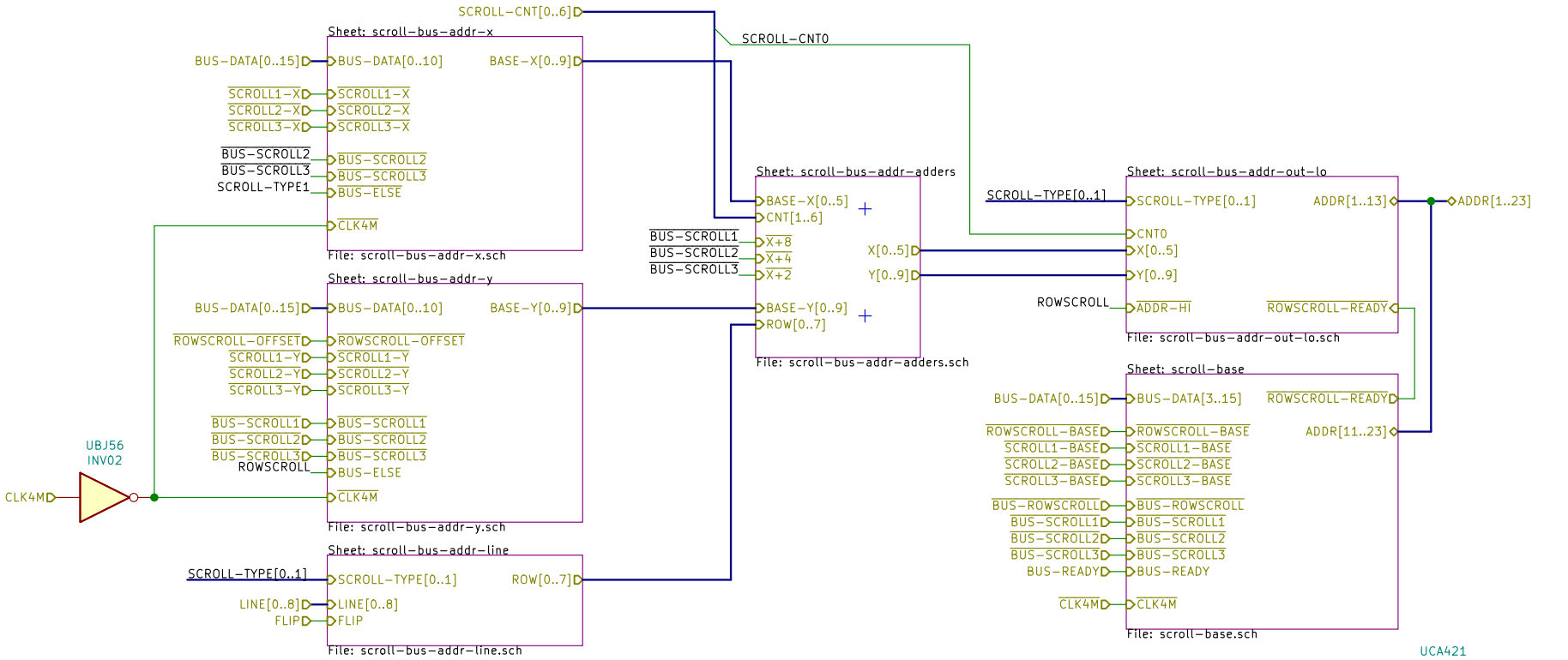
Sheet: /roma-bus/
File: roma-bus.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 10/83



ADDR	SCROLL1	SCROLL2	SCROLL3	ROWSCROLL
23	BASE15	BASE15	BASE15	BASE15
22	BASE14	BASE14	BASE14	BASE14
21	BASE13	BASE13	BASE13	BASE13
20	BASE12	BASE12	BASE12	BASE12
19	BASE11	BASE11	BASE11	BASE11
18	BASE10	BASE10	BASE10	BASE10
17	BASE09	BASE09	BASE09	BASE09
16	BASE08	BASE08	BASE08	BASE08
15	BASE07	BASE07	BASE07	BASE07
14	BASE06	BASE06	BASE06	BASE06
13	Y5	Y5	Y5	BASE05
12	X5	Y4	Y4	BASE04
11	X4	X5	Y3	BASE03
10	X3	X4	X5	Y9
9	X2	X3	X4	Y8
8	X1	X2	X3	Y7
7	X0	X1	X2	Y6
6	Y4	X0	X1	Y5
5	Y3	Y3	X0	Y4
4	Y2	Y2	Y2	Y3
3	Y1	Y1	Y1	Y2
2	Y0	Y0	Y0	Y1
1	ATTR	ATTR	ATTR	Y0

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Sheet: /scroll-bus-addr/
File: scroll-bus-addr.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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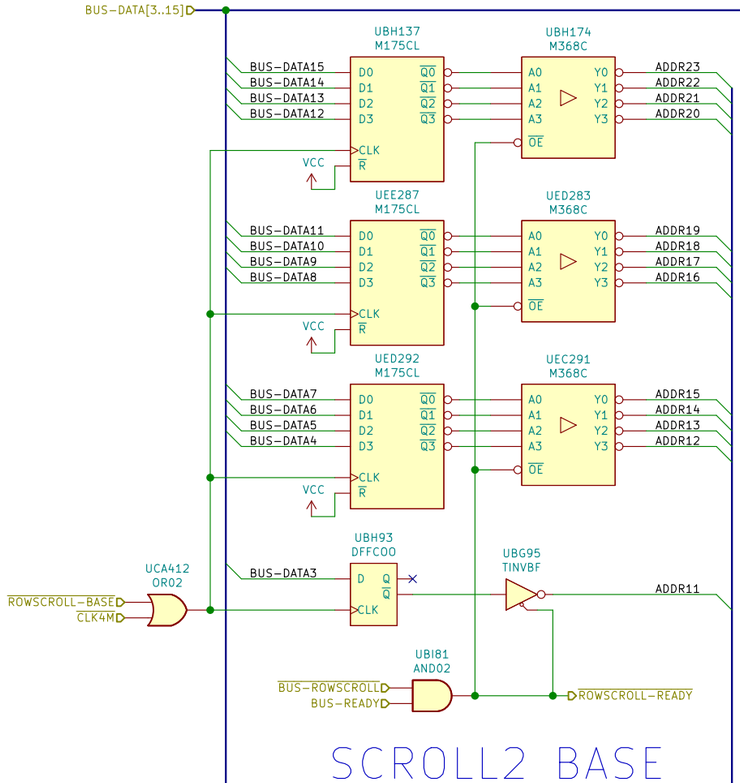
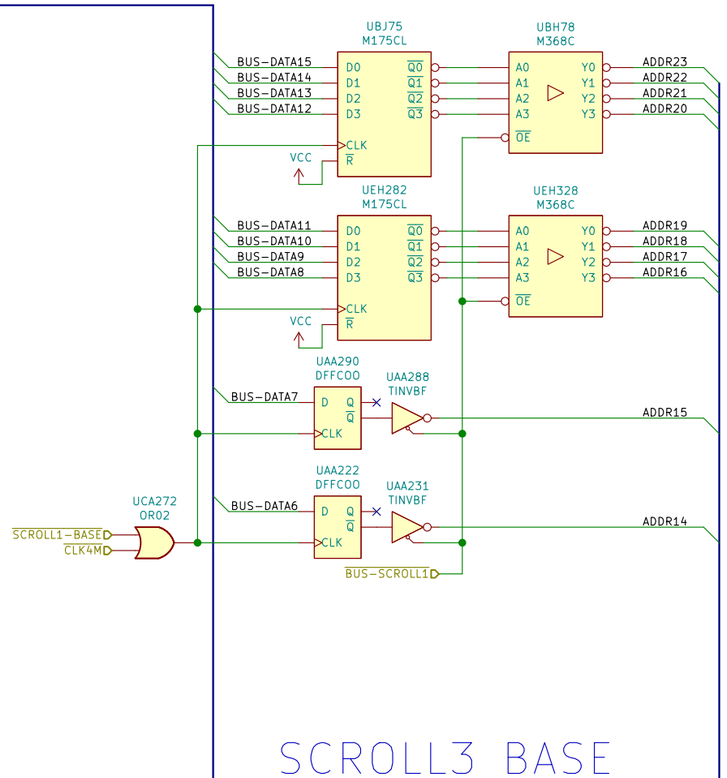
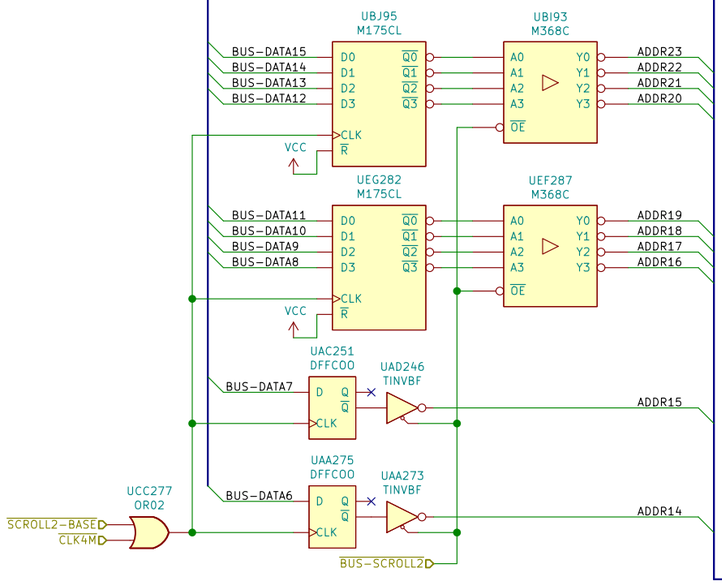
ROWSCROLL BASE



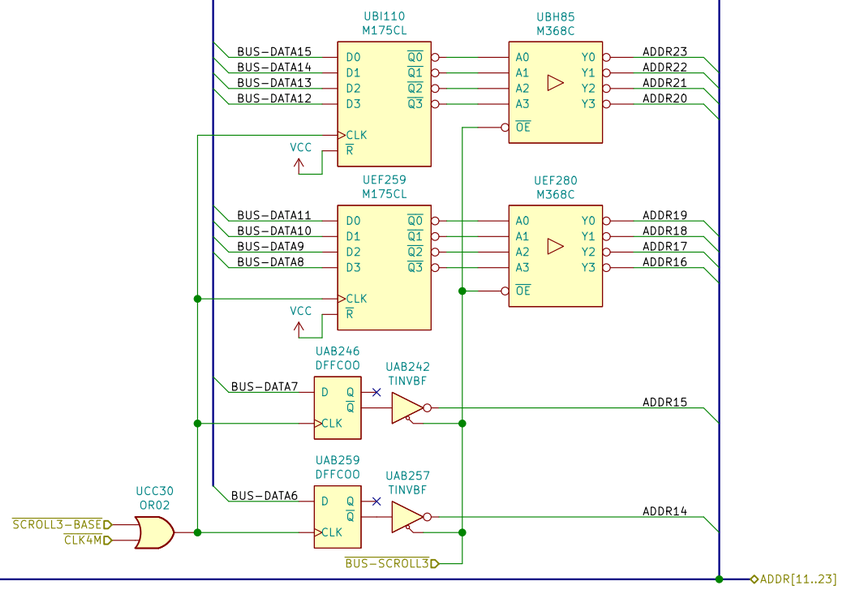
SCROLL1 BASE



SCROLL2 BASE



SCROLL3 BASE



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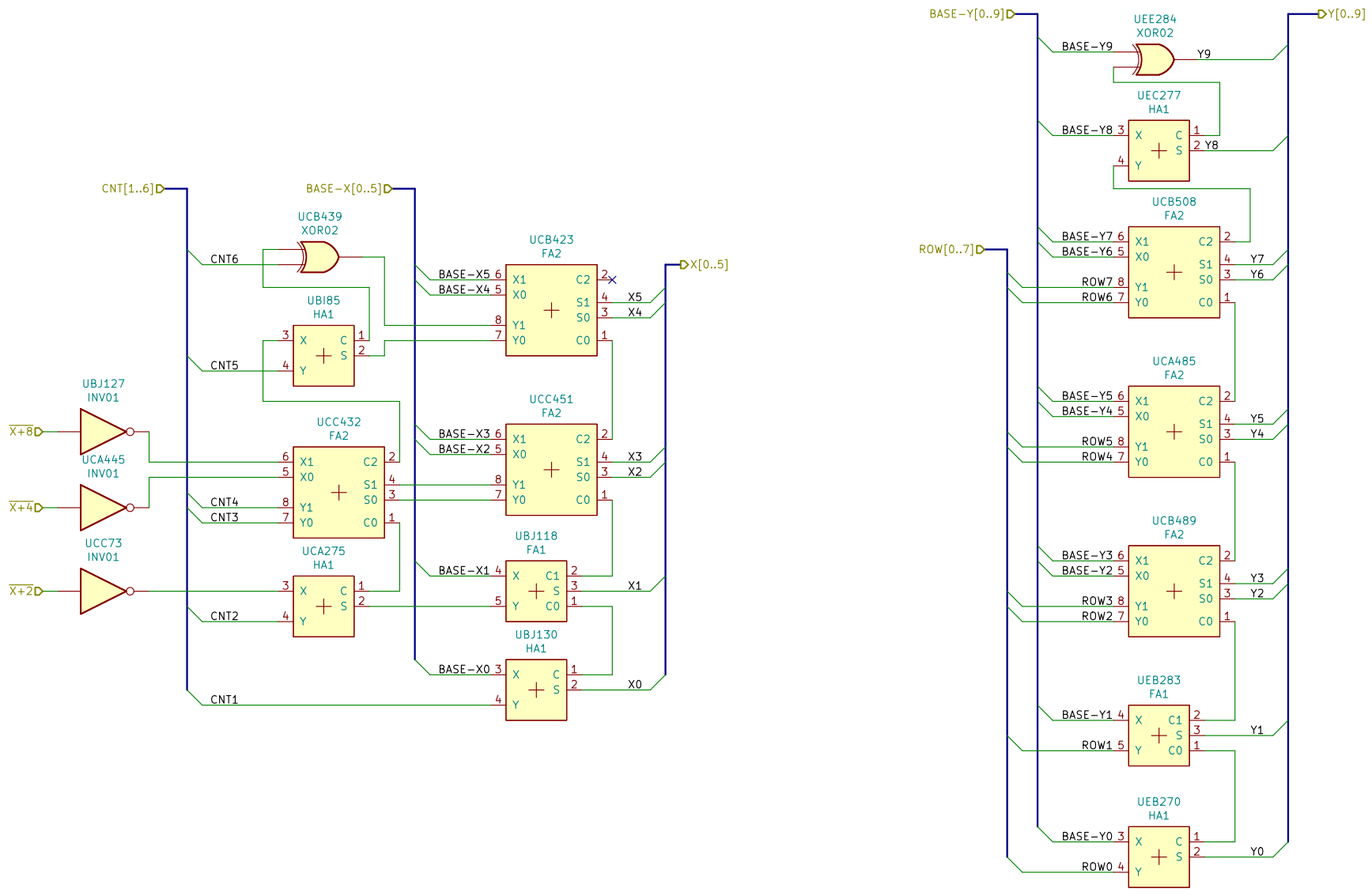
Sheet: /scroll-bus-addr/scroll-base/
File: scroll-base.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 12/83



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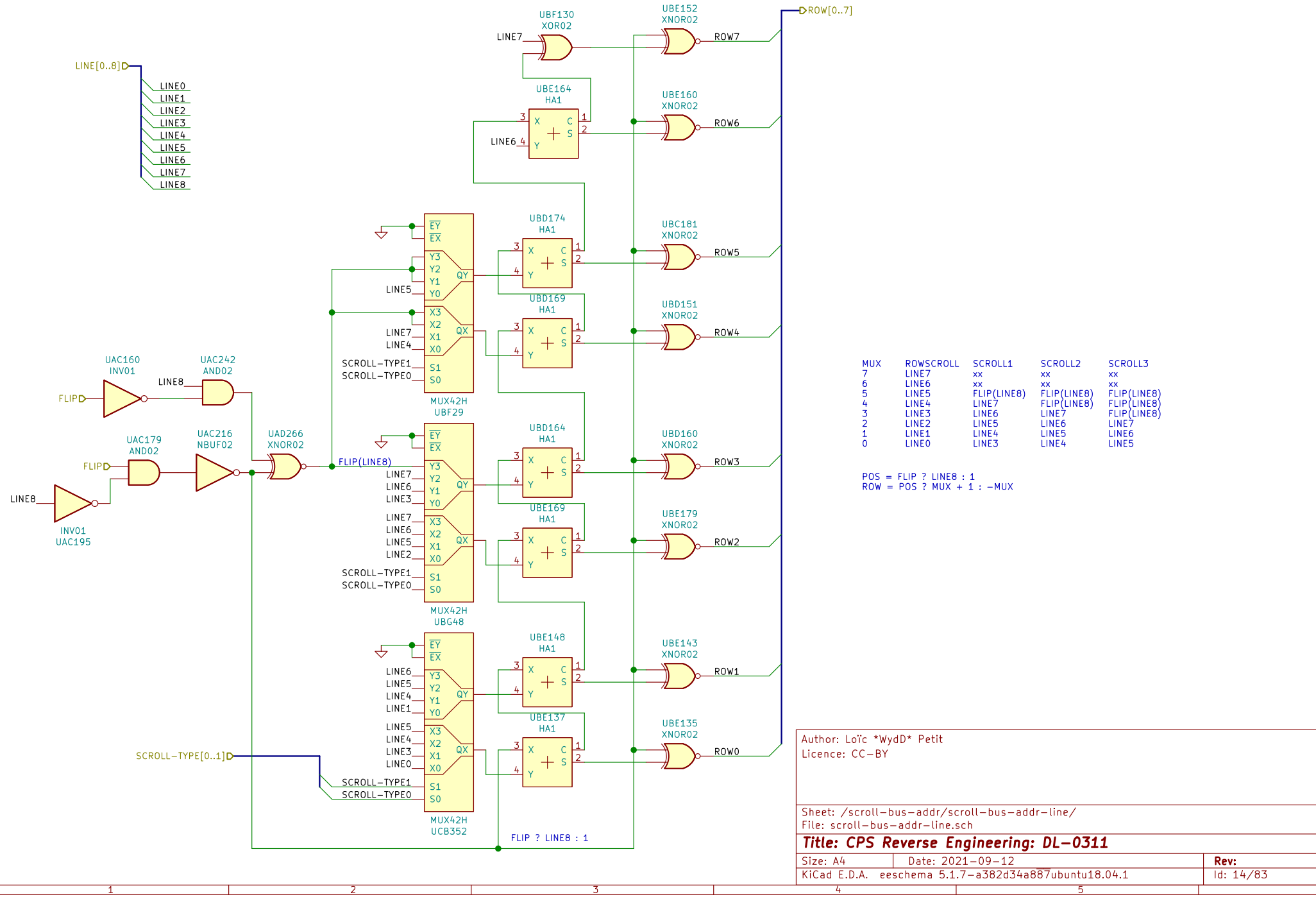
Sheet: /scroll-bus-addr/scroll-bus-addr-adders/
File: scroll-bus-addr-adders.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 13/83



MUX	ROWSCROLL	SCROLL1	SCROLL2	SCROLL3
7	LINE7	xx	xx	xx
6	LINE6	xx	xx	xx
5	LINE5	FLIP(LINE8)	FLIP(LINE8)	FLIP(LINE8)
4	LINE4	LINE7	FLIP(LINE8)	FLIP(LINE8)
3	LINE3	LINE6	LINE7	FLIP(LINE8)
2	LINE2	LINE5	LINE6	LINE7
1	LINE1	LINE4	LINE5	LINE6
0	LINE0	LINE3	LINE4	LINE5

POS = FLIP ? LINE8 : 1
ROW = POS ? MUX + 1 : -MUX

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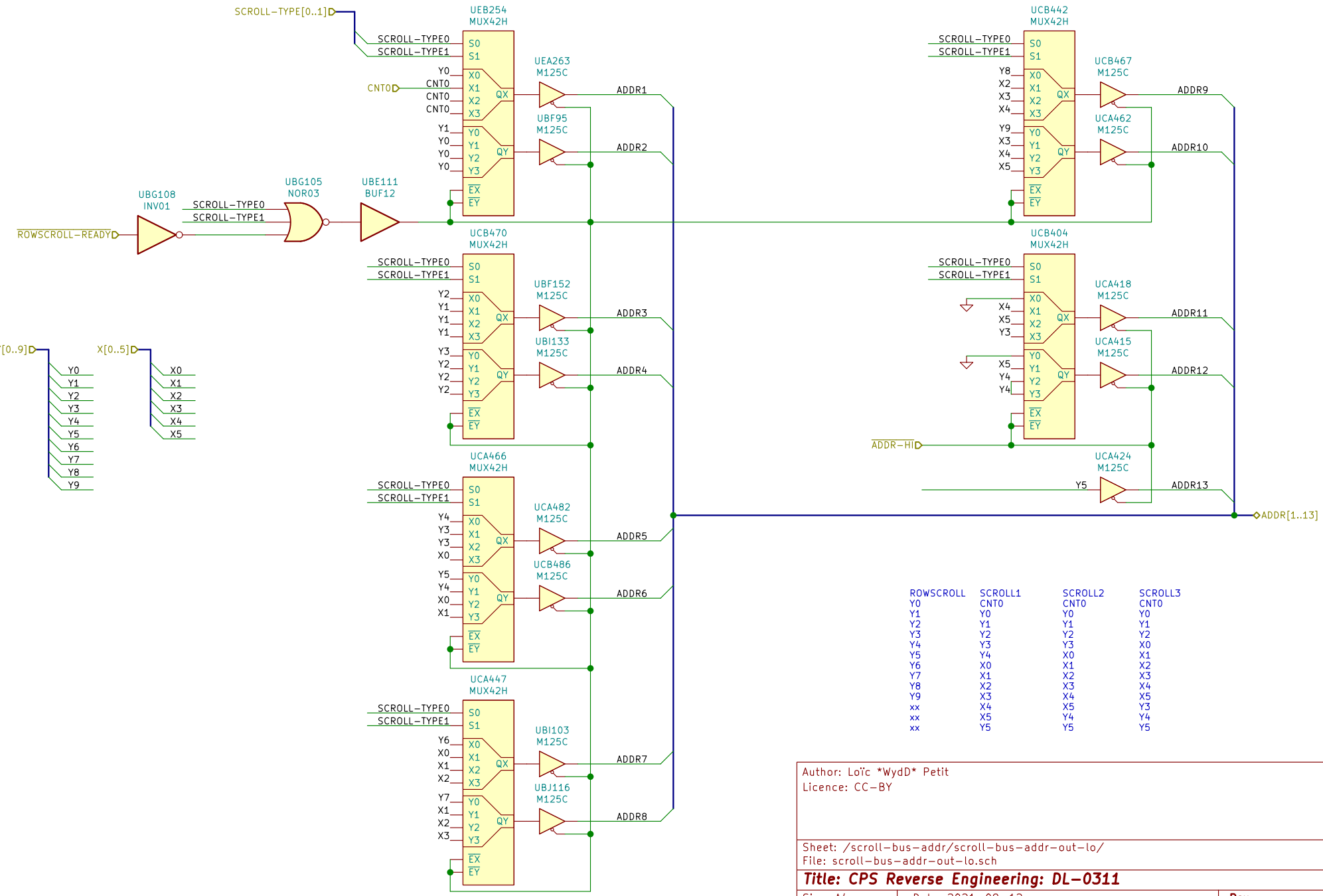
Sheet: /scroll-bus-addr/scroll-bus-addr-line/
File: scroll-bus-addr-line.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 14/83



ROWSCROLL	SCROLL1	SCROLL2	SCROLL3
Y0	CNT0	Y0	CNT0
Y1	Y0	Y1	Y0
Y2	Y1	Y2	Y1
Y3	Y2	Y3	Y2
Y4	Y3	X0	X0
Y5	Y4	X1	X1
Y6	X0	X2	X2
Y7	X1	X3	X3
Y8	X2	X4	X4
Y9	X3	X5	X5
xx	X4	Y4	Y3
xx	X5	Y5	Y4
xx	Y5		Y5

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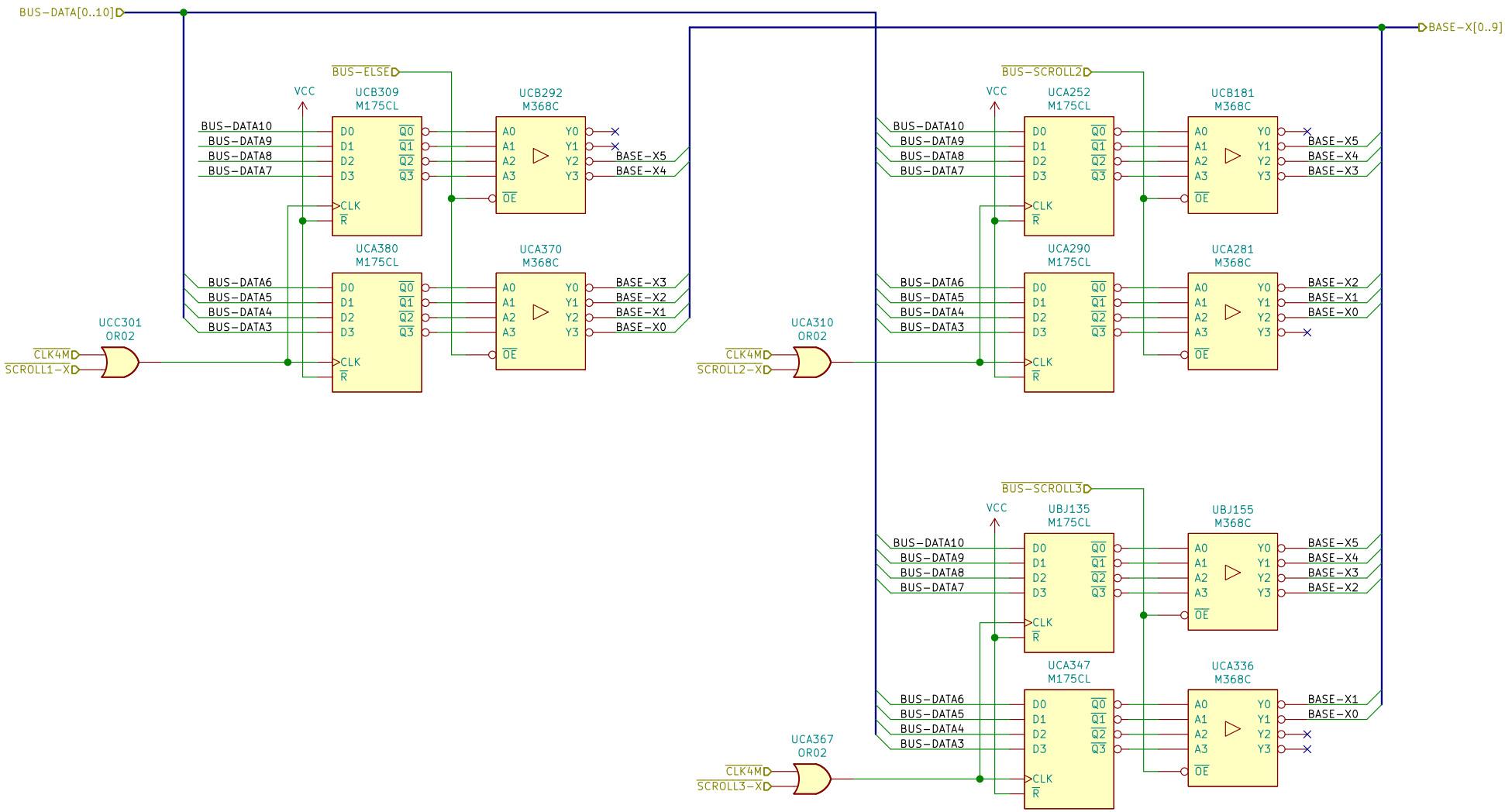
Sheet: /scroll-bus-addr/scroll-bus-addr-out-lo/
File: scroll-bus-addr-out-lo.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 15/83



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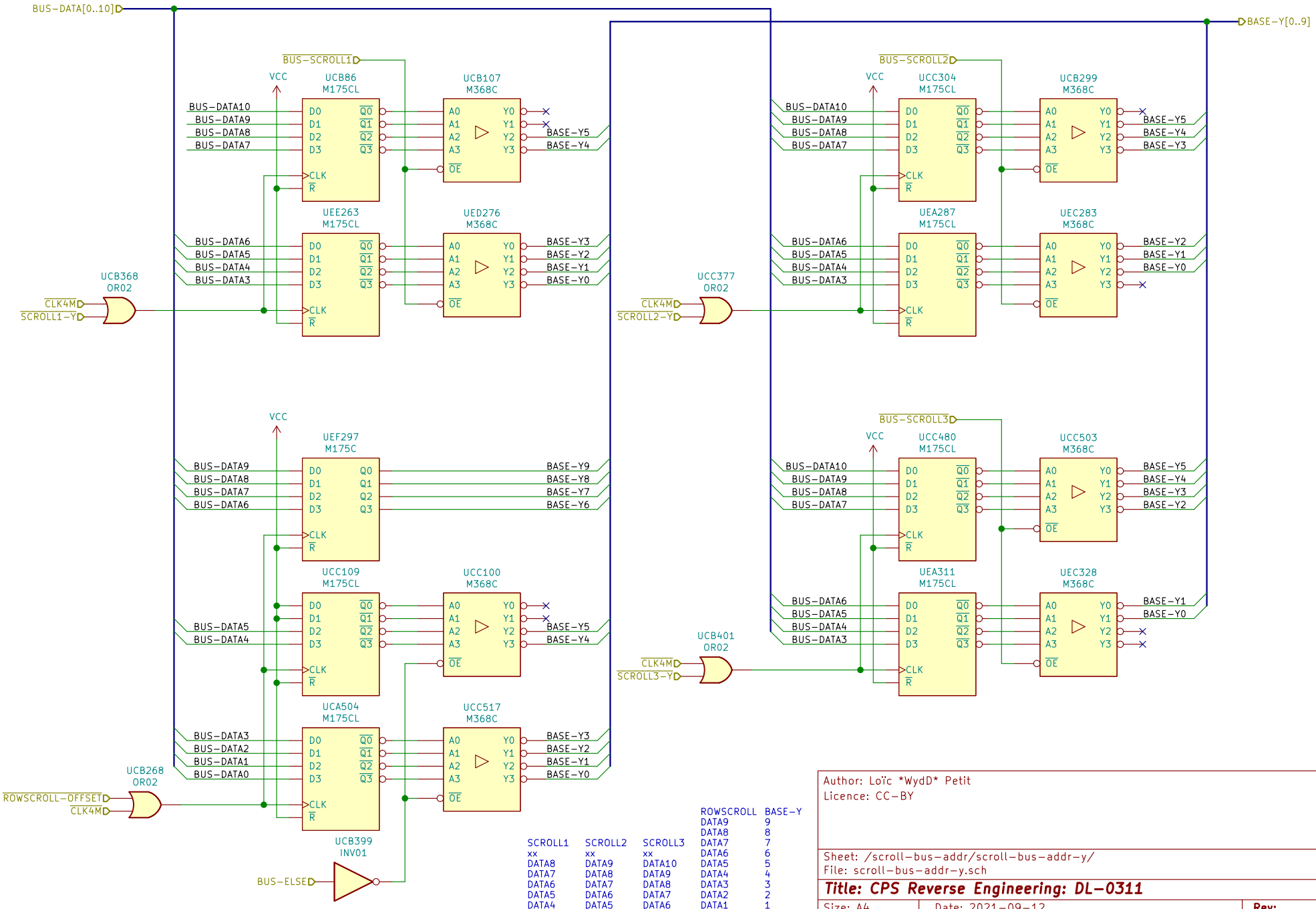
Sheet: /scroll-bus-addr/scroll-bus-addr-x/
File: scroll-bus-addr-x.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 16/83


BUS-DATA[0..10]
BASE-Y[0..9]
BUS-SCROLL1
BUS-SCROLL2
BUS-SCROLL3
VCC
UCB86
M175CL
UCB107
M368C
UEE263
M175CL
UED276
M368C
UCB368
OR02
CLK4M
SCROLL1-Y
UCC304
M175CL
UCB299
M368C
UEA287
M175CL
UEC283
M368C
UCC377
OR02
SCROLL2-Y
UEF297
M175C
UCC109
M175CL
UCC100
M368C
UCA504
M175CL
UCC517
M368C
UCB268
OR02
ROWSCROLL-OFFSET
UCB399
INV01
BUS-ELSE
UCC480
M175CL
UCC503
M368C
UEA311
M175CL
UEC328
M368C
UCB401
OR02
SCROLL3-Y
BUS-DATA10
BUS-DATA9
BUS-DATA8
BUS-DATA7
BUS-DATA6
BUS-DATA5
BUS-DATA4
BUS-DATA3
BUS-DATA2
BUS-DATA1
BUS-DATA0
BASE-Y0
BASE-Y1
BASE-Y2
BASE-Y3
BASE-Y4
BASE-Y5
BASE-Y6
BASE-Y7
BASE-Y8
BASE-Y9
SCROLL1 SCROLL2 SCROLL3
xx xx xx
DATA8 DATA9 DATA10
DATA7 DATA8 DATA9
DATA6 DATA7 DATA8
DATA5 DATA6 DATA7
DATA4 DATA5 DATA6
DATA3 DATA4 DATA5
ROWSCROLL BASE-Y
DATA9 9
DATA8 8
DATA7 7
DATA6 6
DATA5 5
DATA4 4
DATA3 3
DATA2 2
DATA1 1
DATA0 0
Author: Loïc *WydD* Petit
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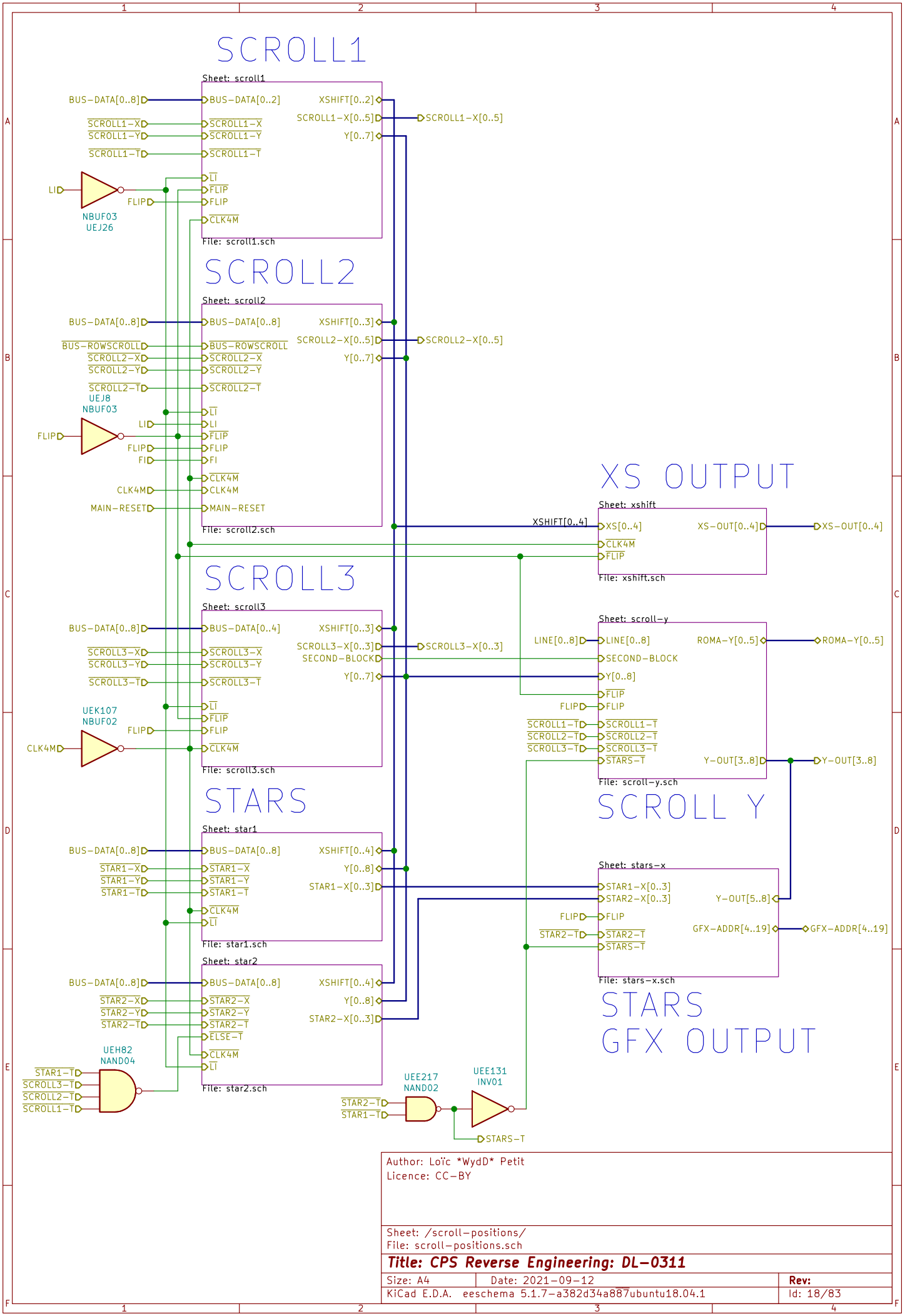
Sheet: /scroll-bus-addr/scroll-bus-addr-y/
File: scroll-bus-addr-y.sch
Title: CPS Reverse Engineering: DL-0311
Size: A4
Date: 2021-09-12
Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1
Id: 17/83


SCROLL1
Sheet: scroll1
BUS-DATA[0..8]
BUS-DATA[0..2]
XSHIFT[0..2]
SCROLL1-X[0..5]
SCROLL1-X[0..5]
SCROLL1-X
SCROLL1-Y
SCROLL1-T
Y[0..7]
LI
FLIP
CLK4M
NBUF03
UEJ26
File: scroll1.sch
SCROLL2
Sheet: scroll2
BUS-DATA[0..8]
BUS-ROWSCROLL
SCROLL2-X
SCROLL2-Y
SCROLL2-T
XSHIFT[0..3]
SCROLL2-X[0..5]
SCROLL2-X[0..5]
Y[0..7]
UEJ8
NBUF03
FI
MAIN-RESET
File: scroll2.sch
XS OUTPUT
Sheet: xshift
XSHIFT[0..4]
XS[0..4]
XS-OUT[0..4]
XS-OUT[0..4]
File: xshift.sch
SCROLL3
Sheet: scroll3
BUS-DATA[0..4]
SCROLL3-X
SCROLL3-Y
SCROLL3-T
XSHIFT[0..3]
SCROLL3-X[0..3]
SCROLL3-X[0..3]
SECOND-BLOCK
UEK107
NBUF02
File: scroll3.sch
Sheet: scroll-y
LINE[0..8]
ROMA-Y[0..5]
ROMA-Y[0..5]
SECOND-BLOCK
Y[0..8]
SCROLL1-T
SCROLL2-T
SCROLL3-T
STARS-T
Y-OUT[3..8]
Y-OUT[3..8]
File: scroll-y.sch
SCROLL Y
STARS
Sheet: star1
BUS-DATA[0..8]
STAR1-X
STAR1-Y
STAR1-T
XSHIFT[0..4]
Y[0..8]
STAR1-X[0..3]
File: star1.sch
Sheet: star2
BUS-DATA[0..8]
STAR2-X
STAR2-Y
STAR2-T
XSHIFT[0..4]
Y[0..8]
STAR2-X[0..3]
ELSE-T
UEH82
NAND04
STAR1-T
SCROLL3-T
SCROLL2-T
SCROLL1-T
File: star2.sch
Sheet: stars-x
STAR1-X[0..3]
STAR2-X[0..3]
Y-OUT[5..8]
STAR2-T
STARS-T
GFX-ADDR[4..19]
GFX-ADDR[4..19]
File: stars-x.sch
STARS
GFX OUTPUT
UEE217
NAND02
UEE131
INV01
STAR2-T
STAR1-T
STARS-T
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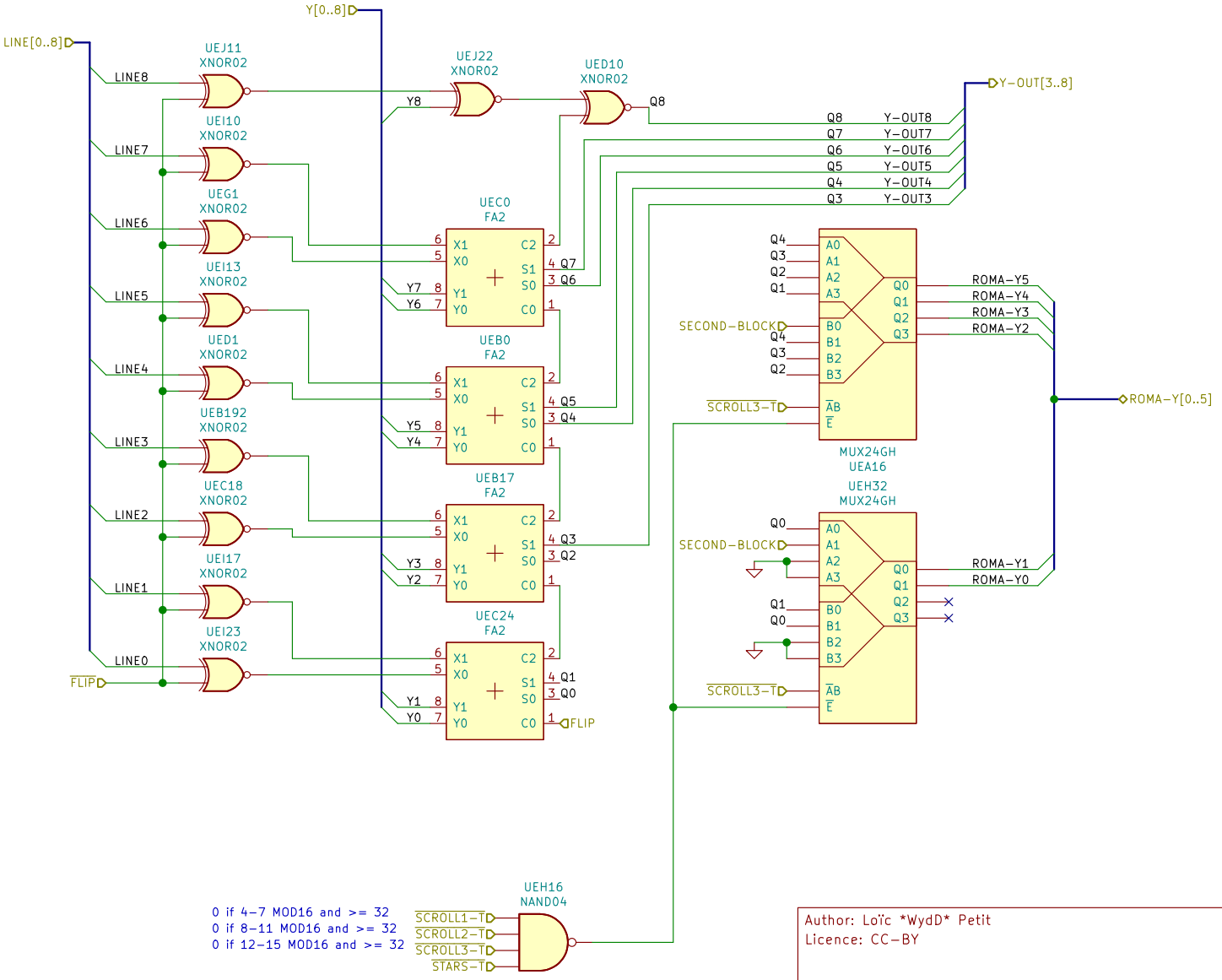
Sheet: /scroll-positions/
File: scroll-positions.sch
Title: CPS Reverse Engineering: DL-0311
Size: A4
Date: 2021-09-12
Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1
Id: 18/83



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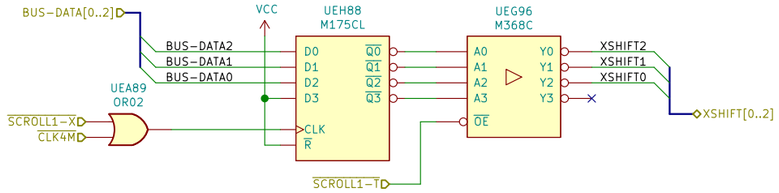
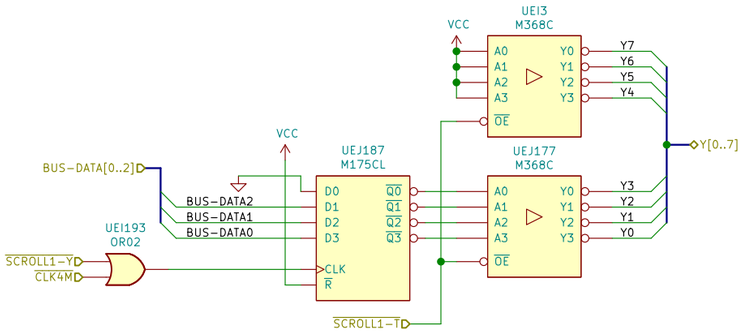
Sheet: /scroll-positions/scroll-y/
File: scroll-y.sch

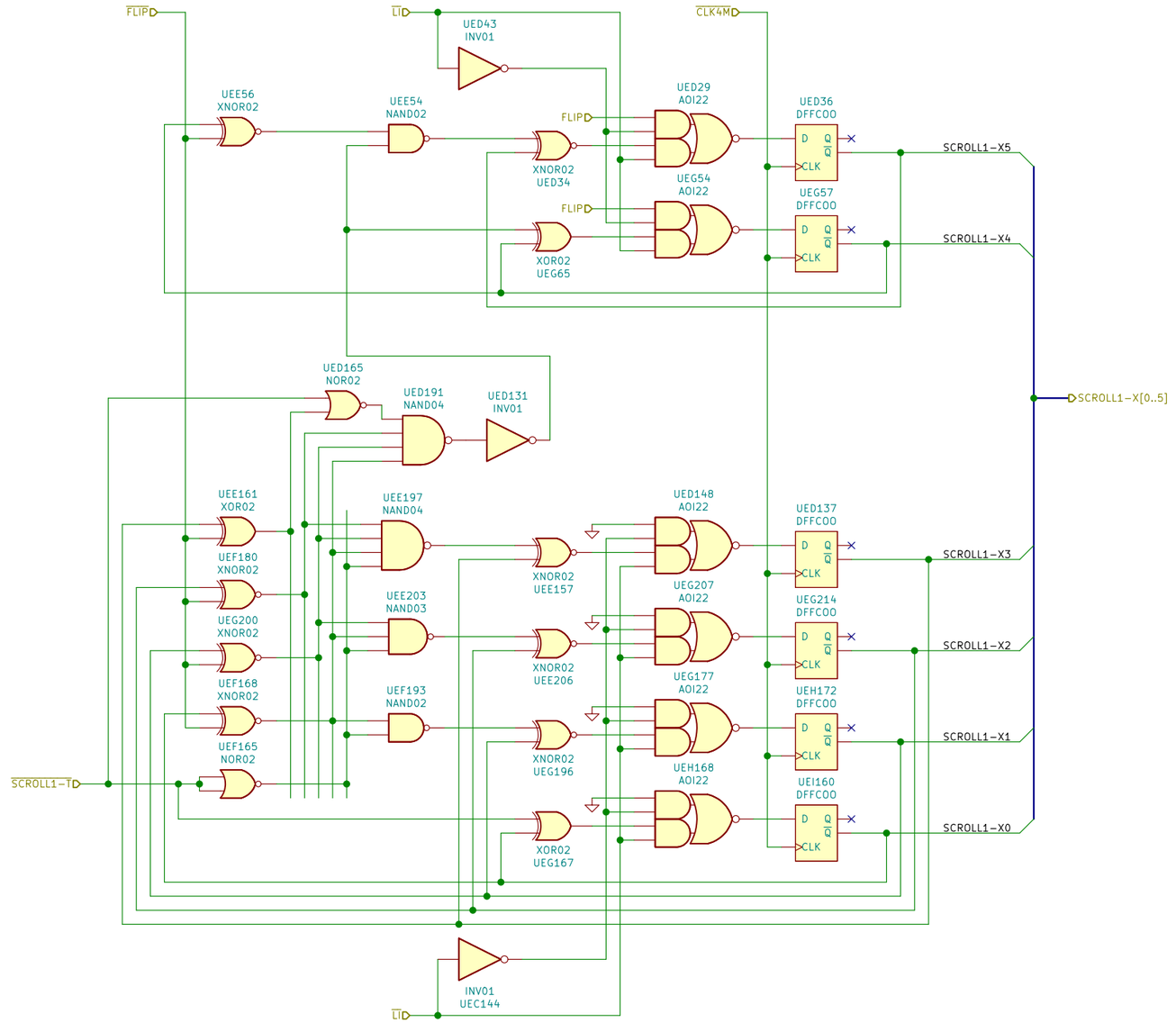
Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 19/83





Y[0..7] BUS



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Sheet: /scroll-positions/scroll1/
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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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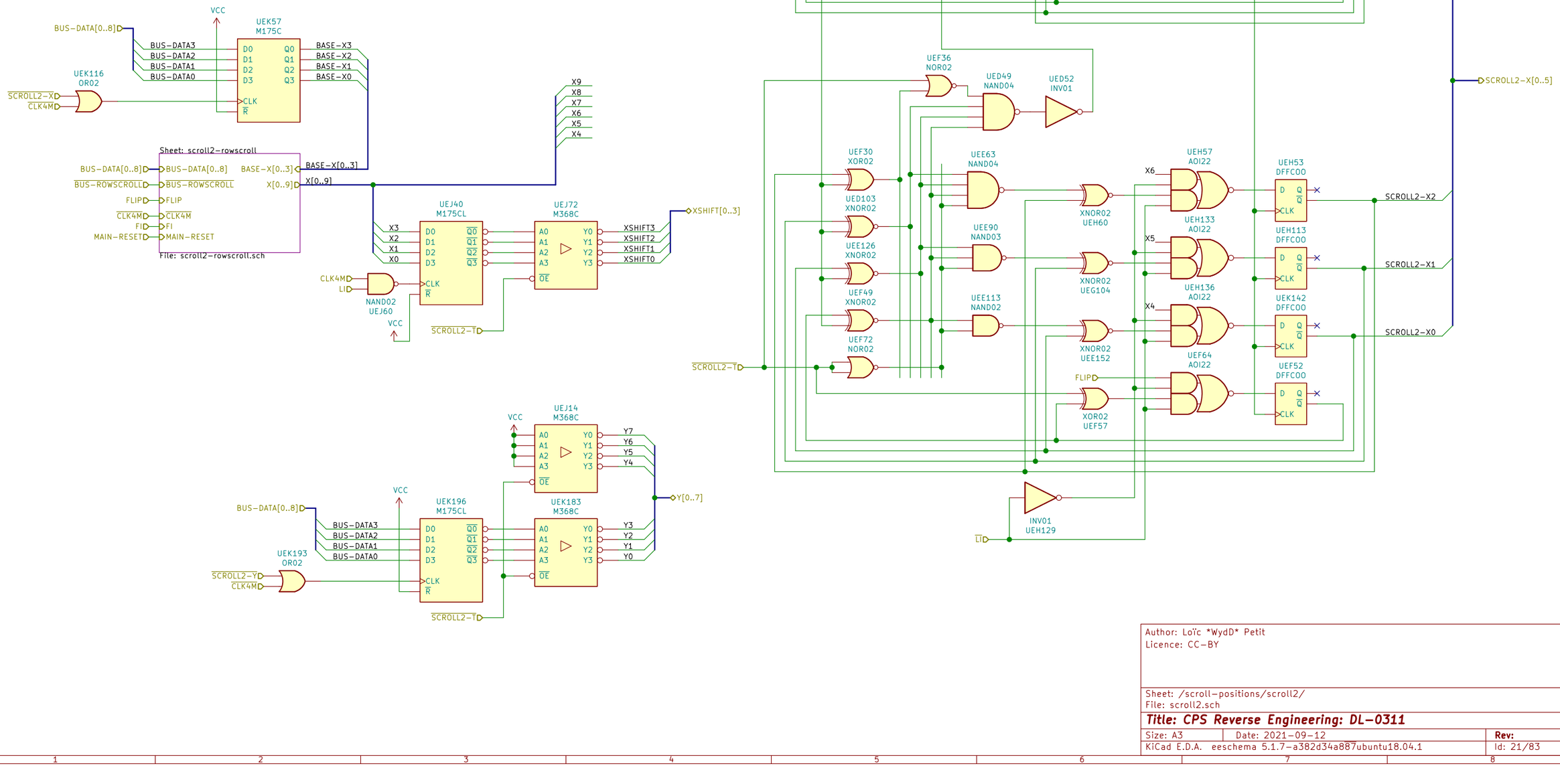

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Sheet: /scroll-positions/scroll2/
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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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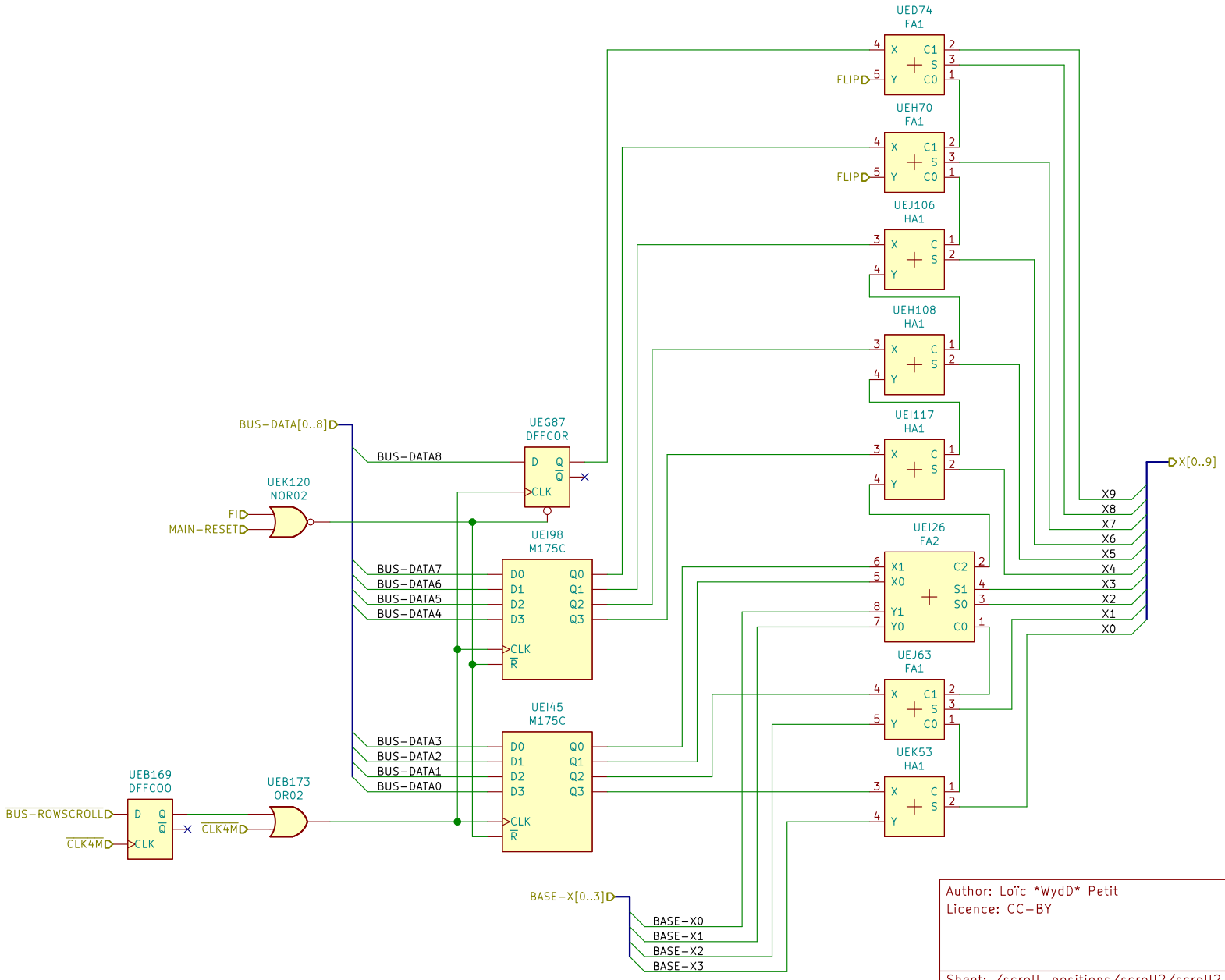

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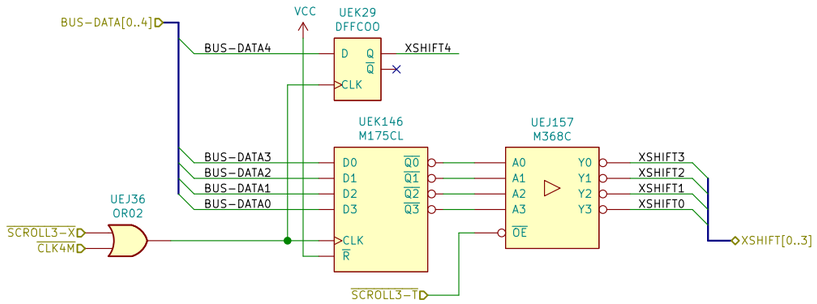
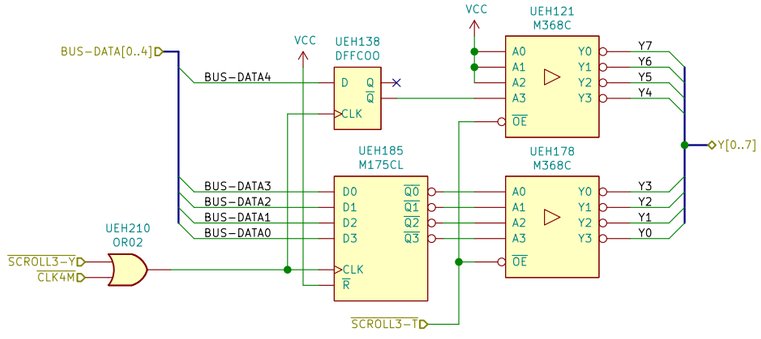
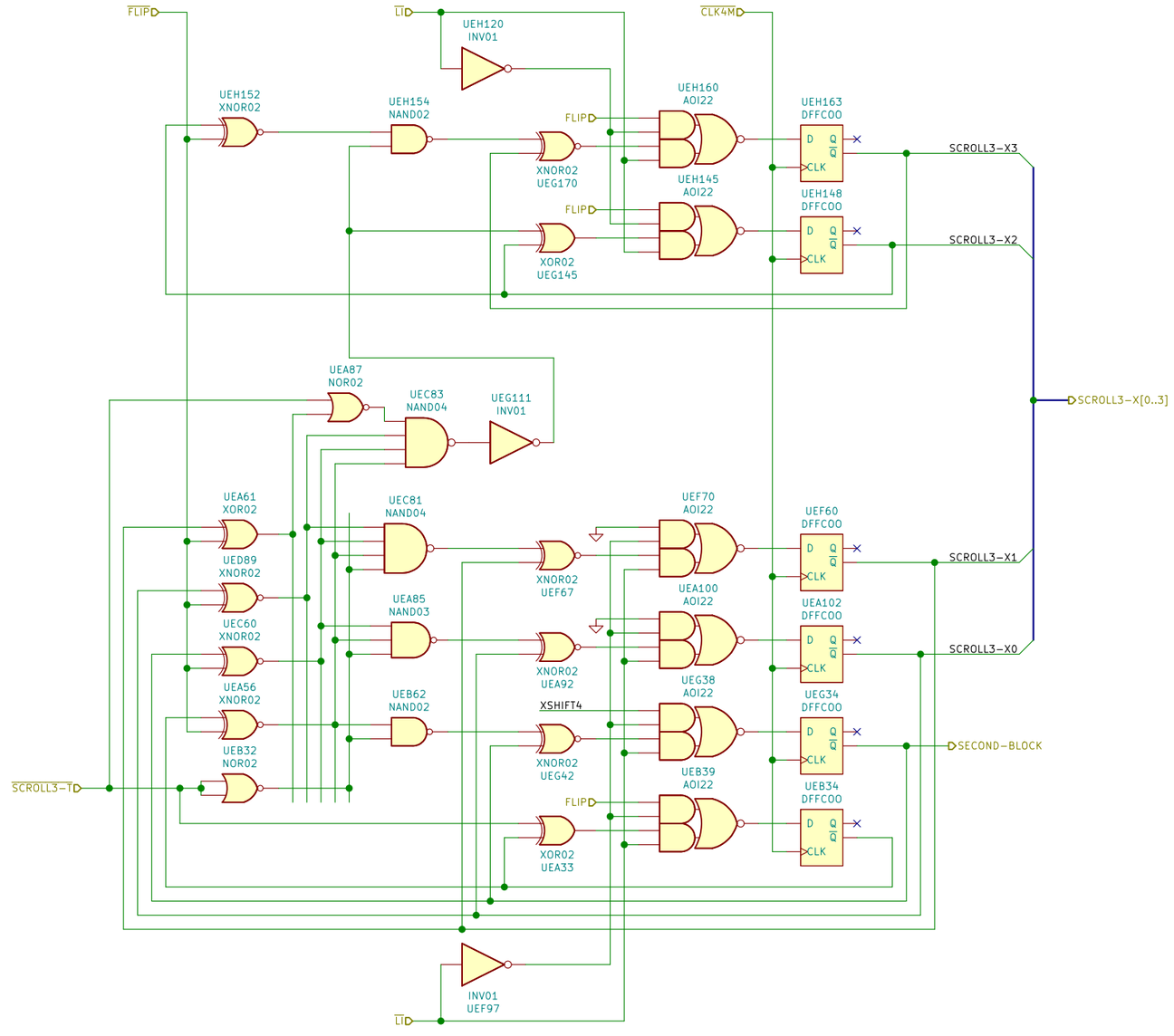
Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 22/83







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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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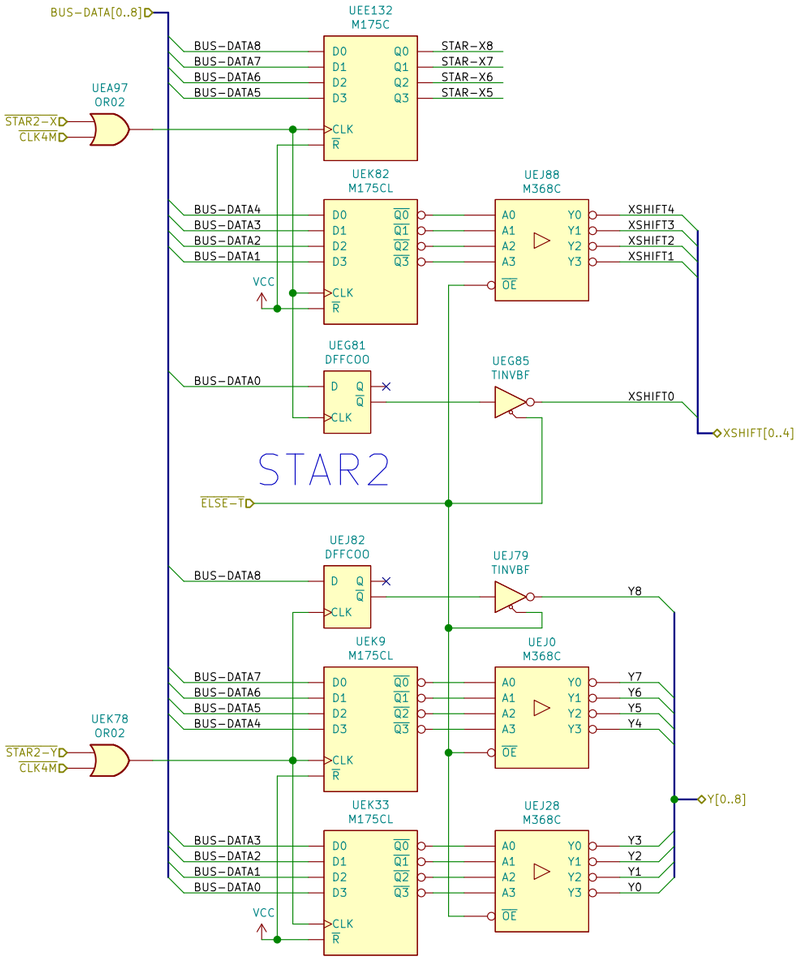

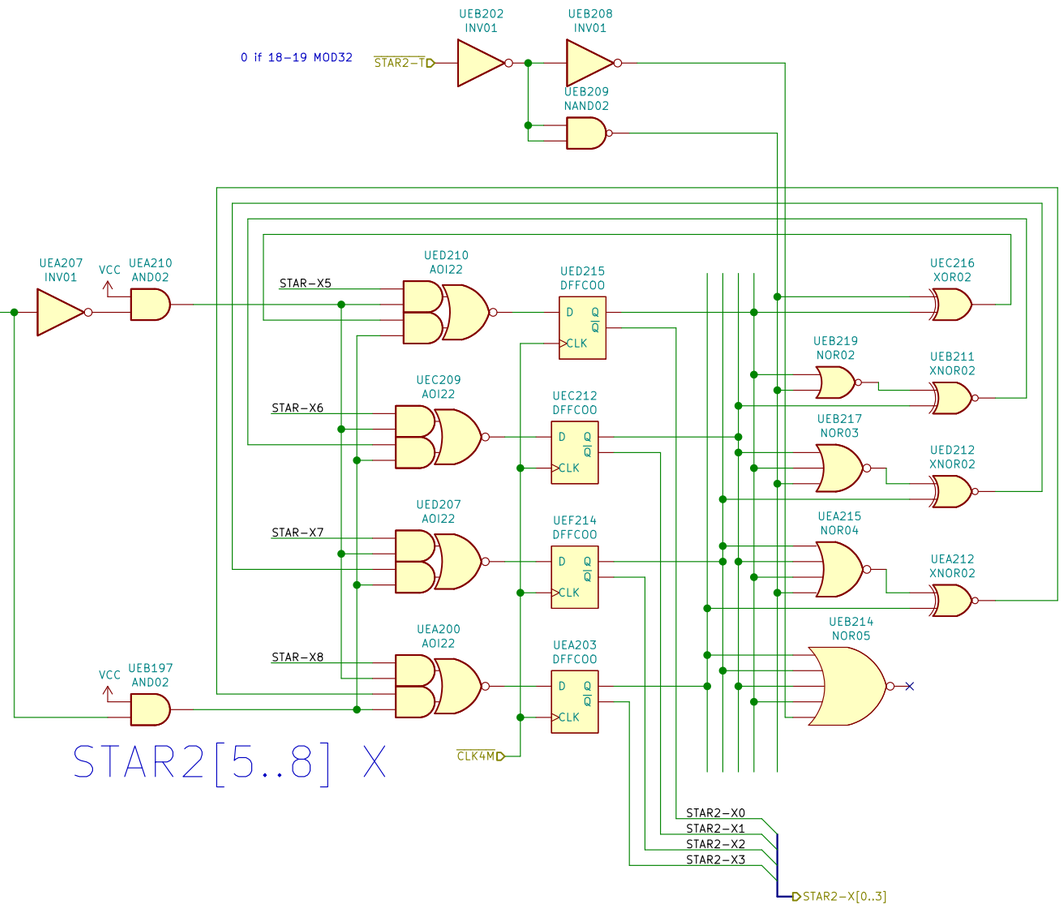

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Sheet: /scroll-positions/star2/
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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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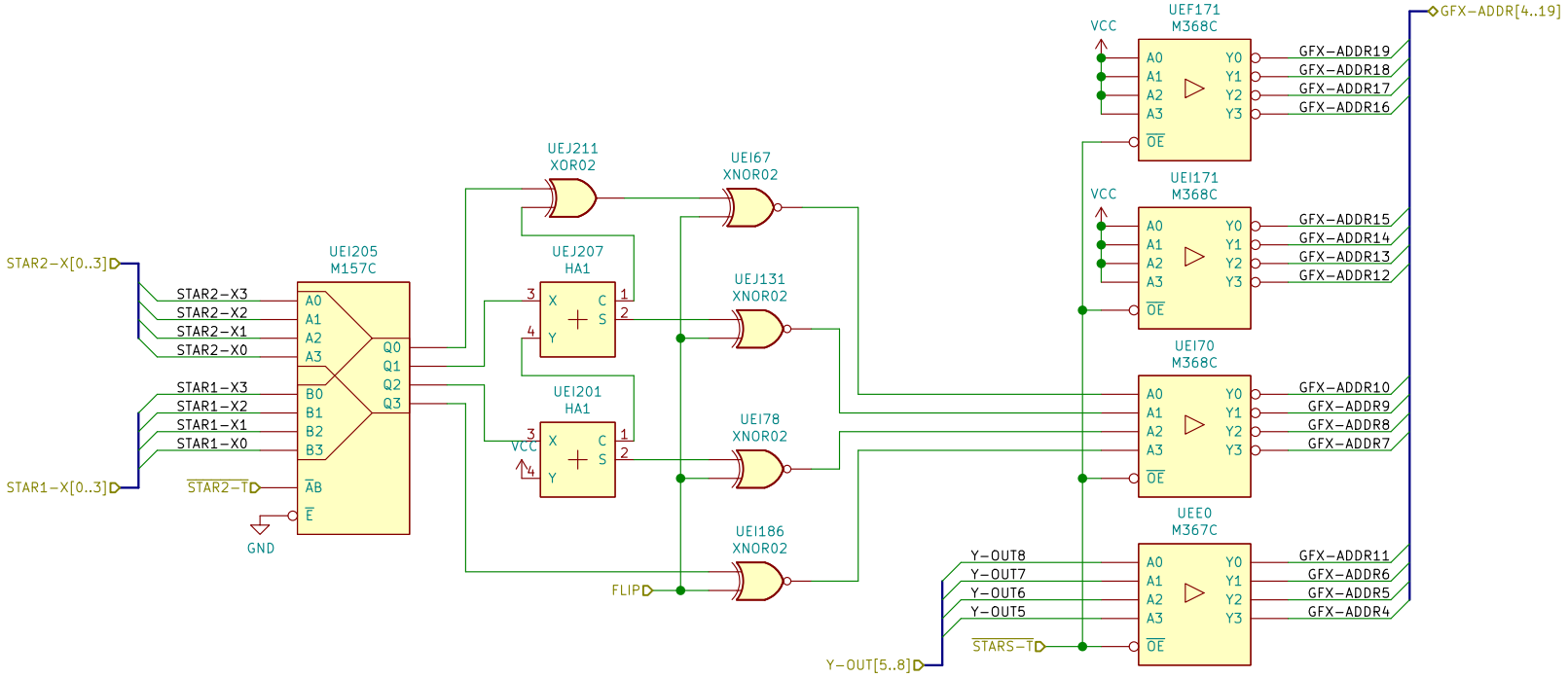

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Sheet: /scroll-positions/stars-x/
File: stars-x.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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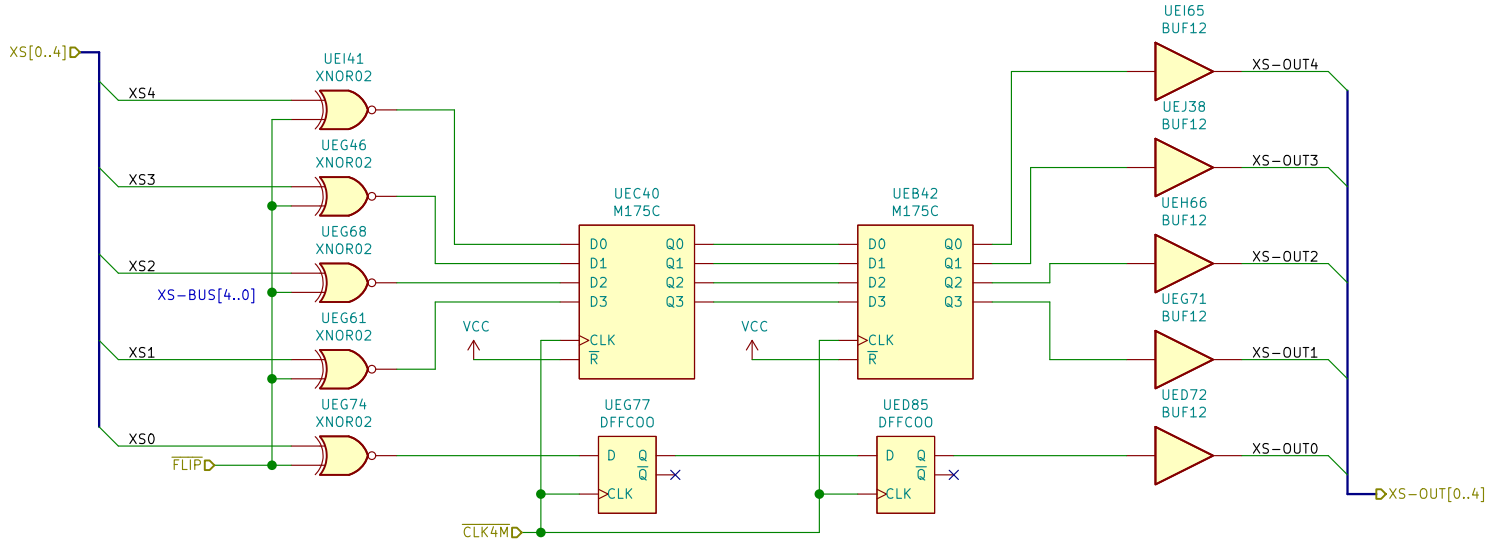

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Sheet: /scroll-positions/xshift/
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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
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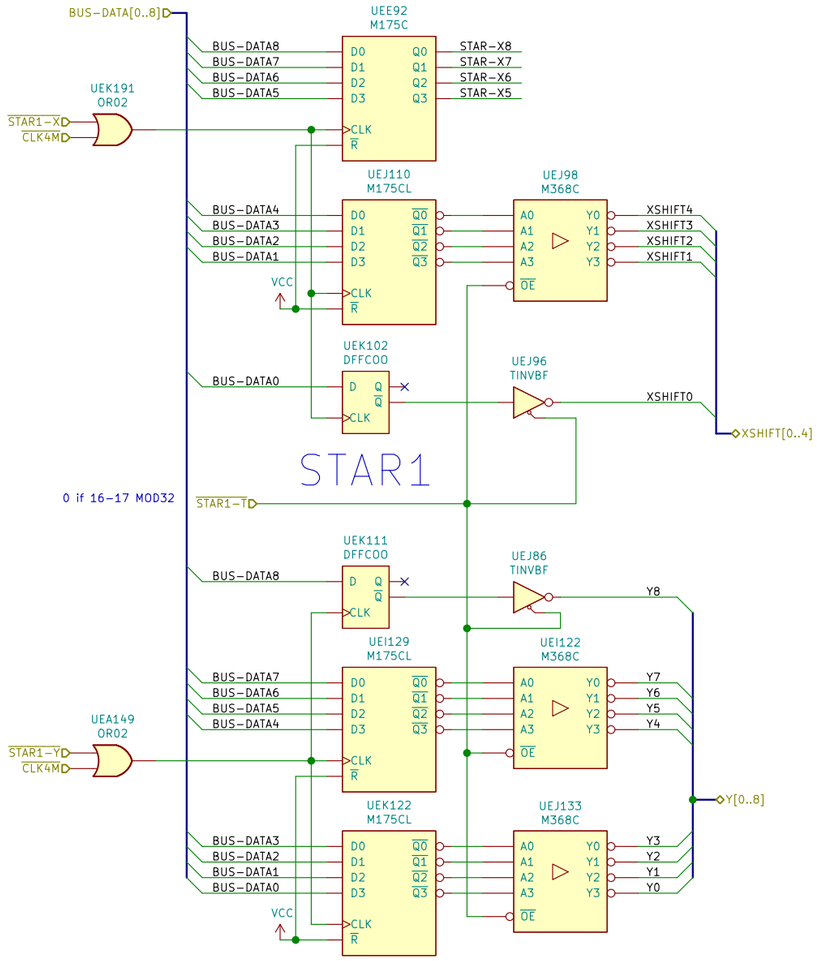

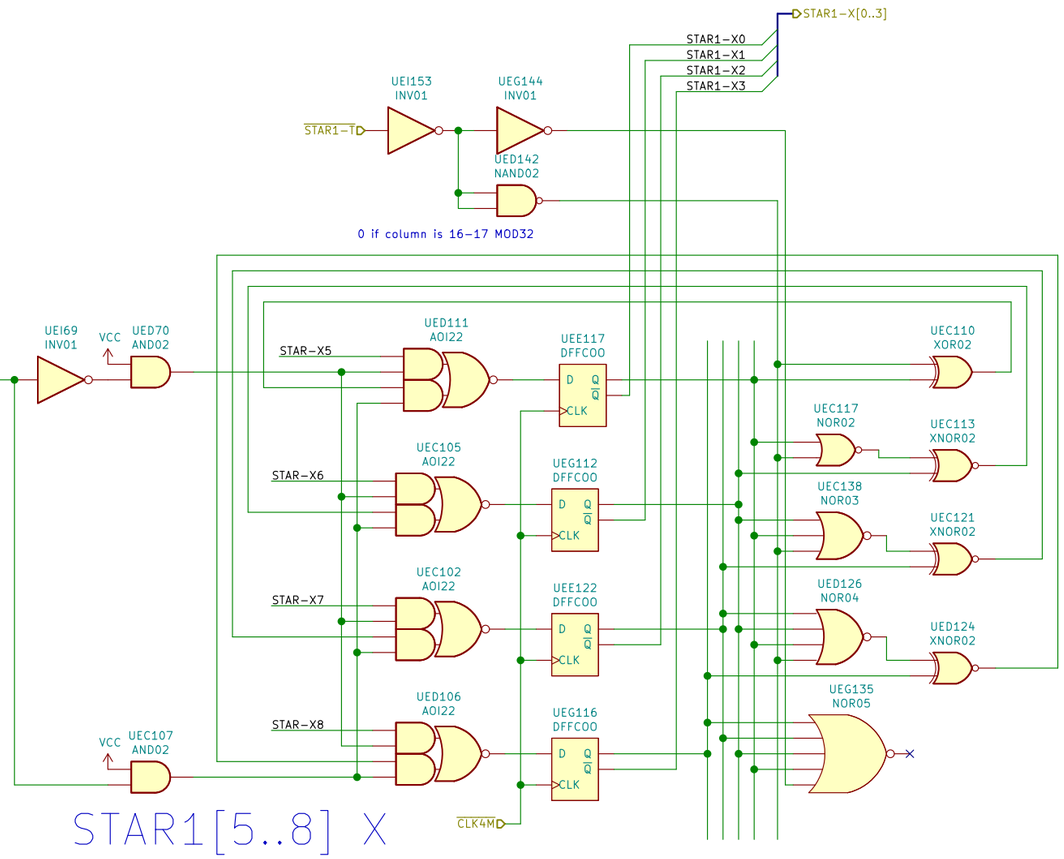

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Sheet: /scroll-positions/star1/
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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
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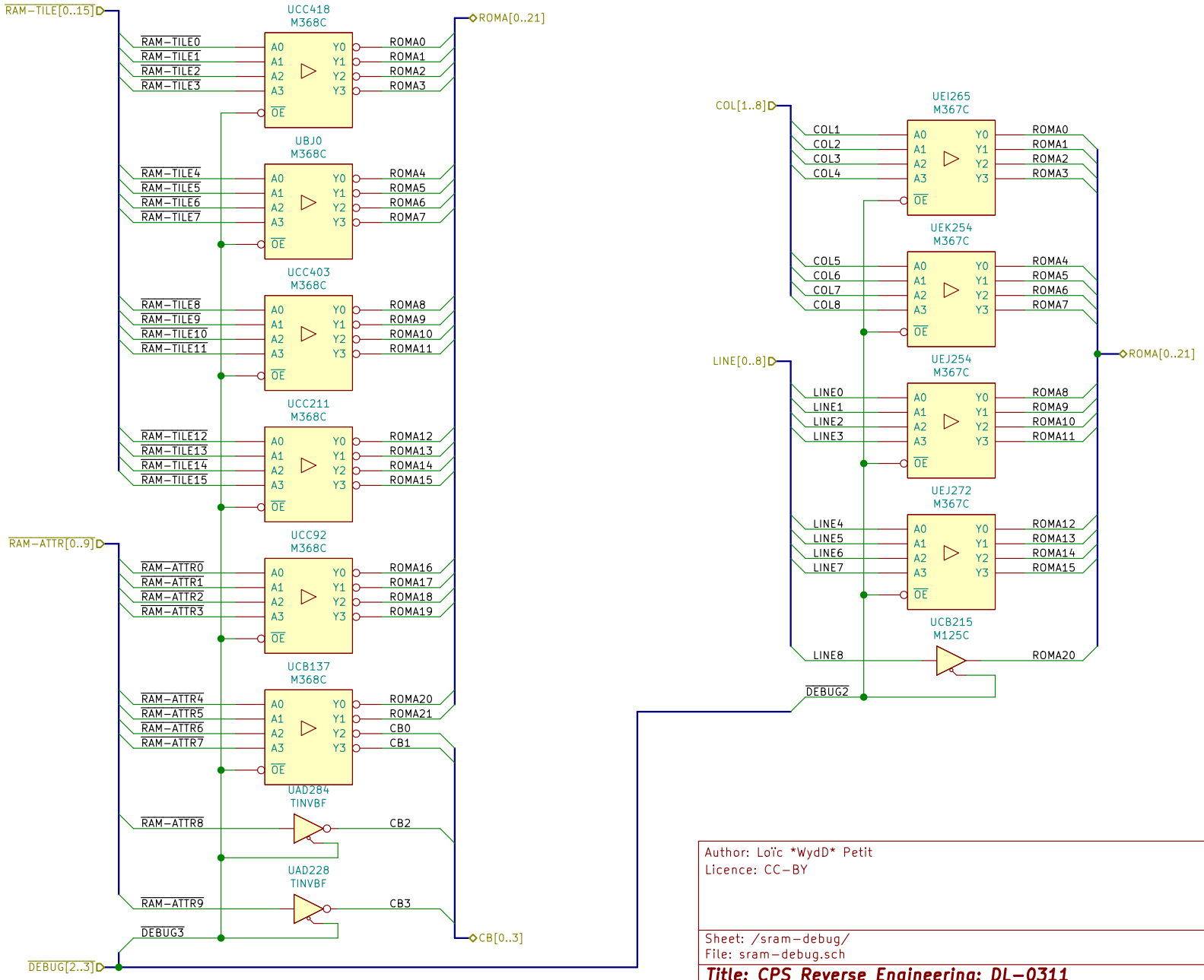

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Sheet: /sram-debug/
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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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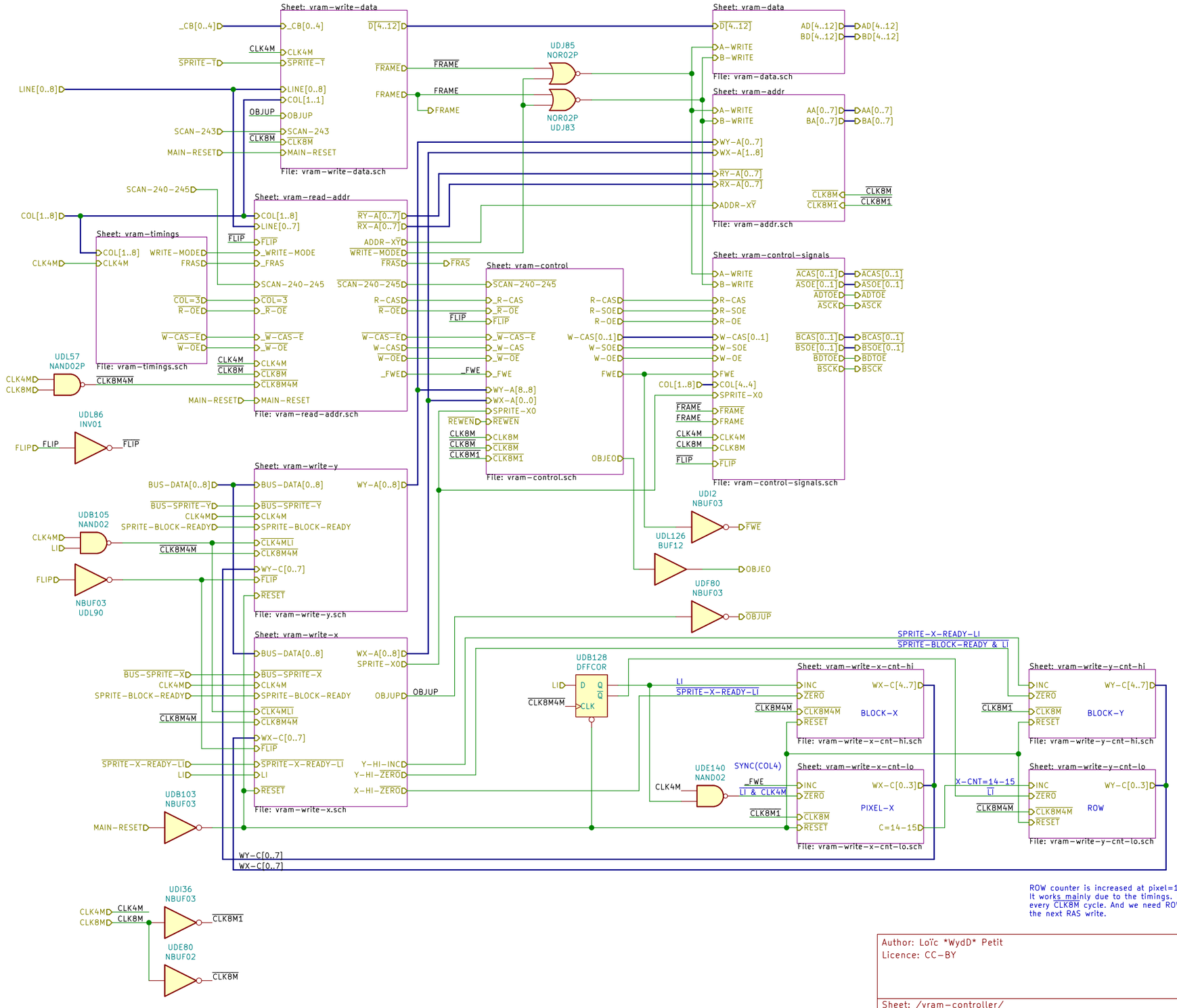

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Sheet: /vram-controller/
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Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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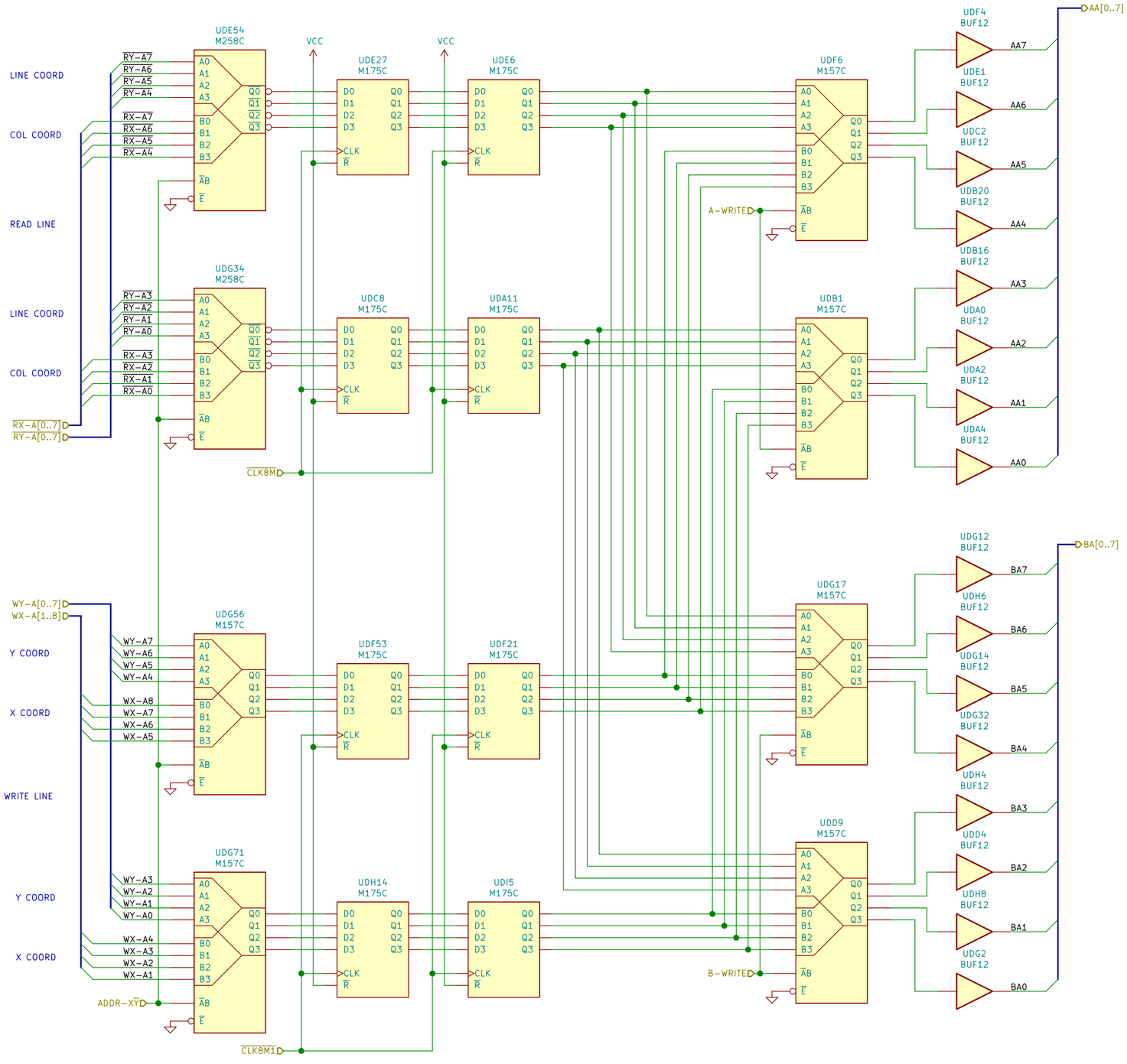

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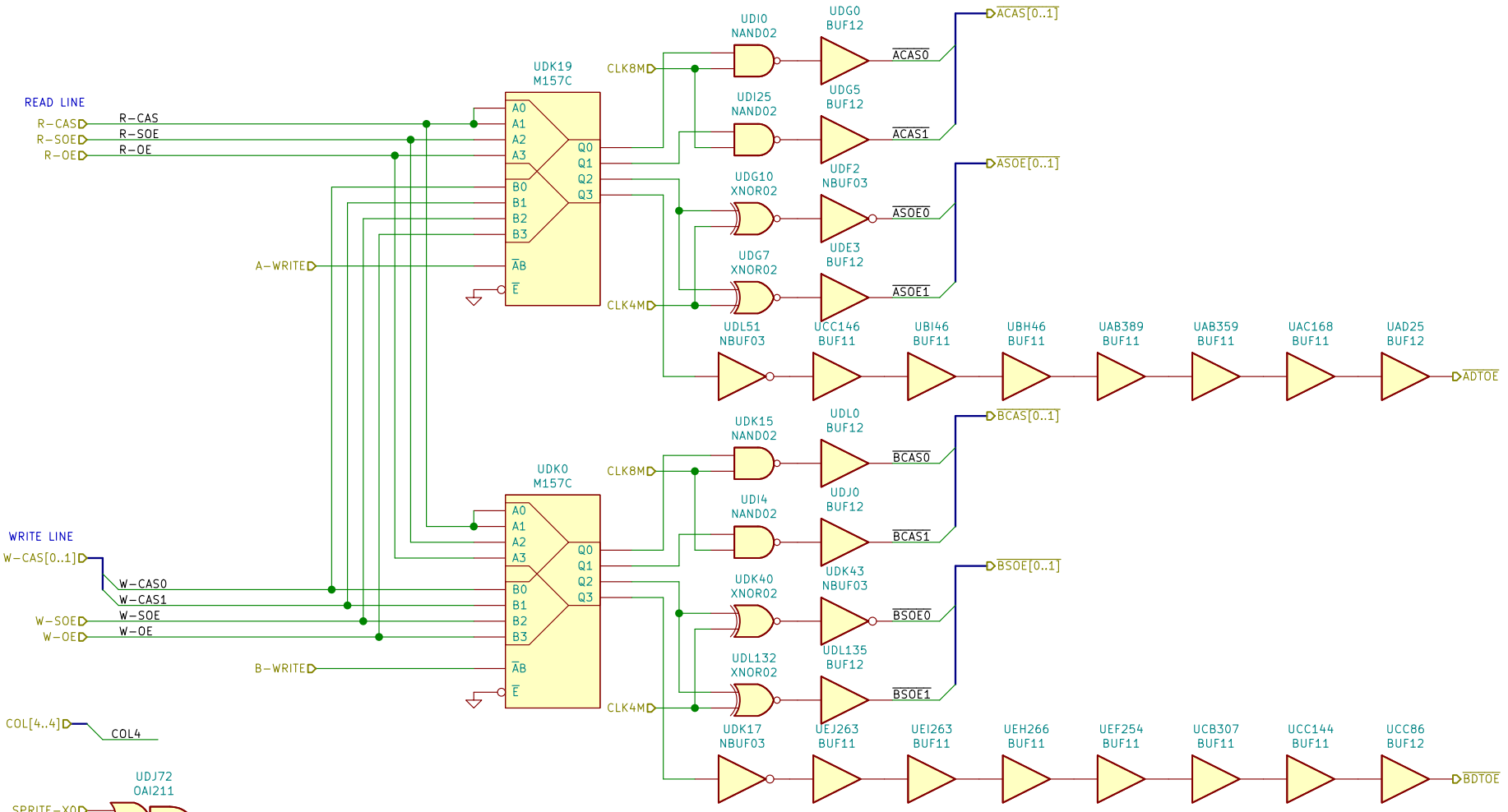
Sheet: /vram-controller/vram-addr/
File: vram-addr.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 30/83



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Title: CPS Reverse Engineering: DL-0311

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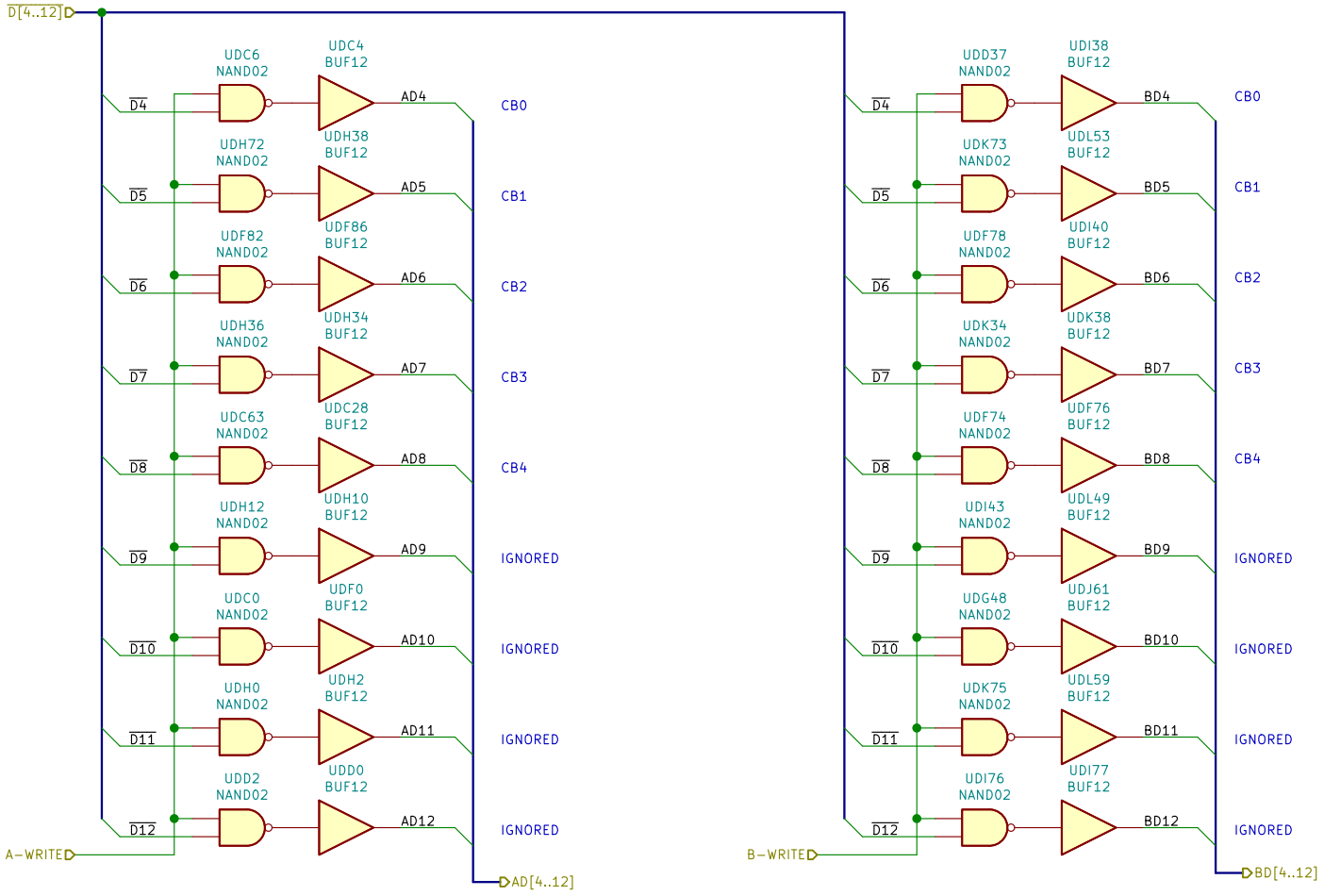

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Sheet: /vram-controller/vram-data/
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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
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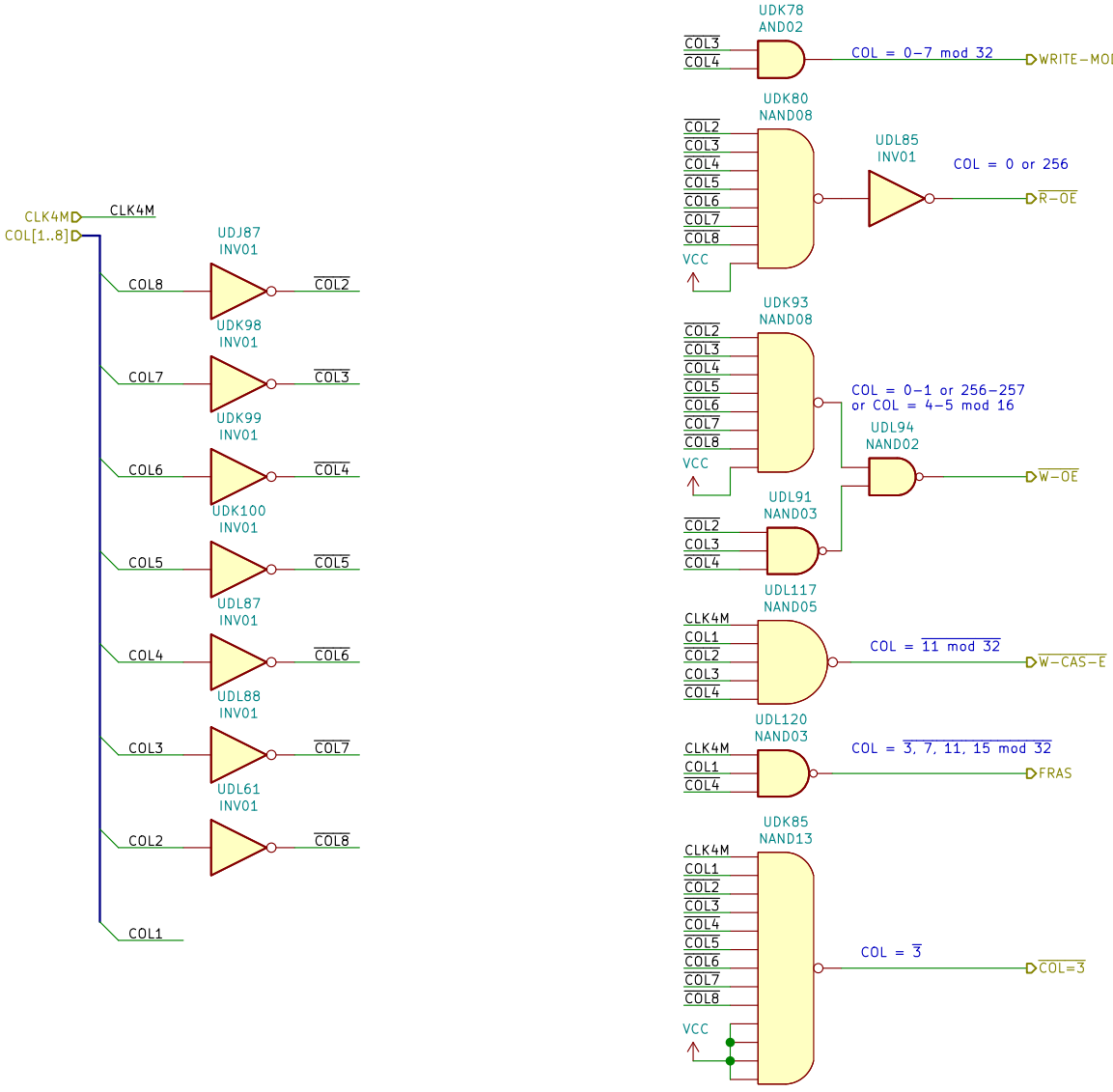

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Sheet: /vram-controller/vram-timings/
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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
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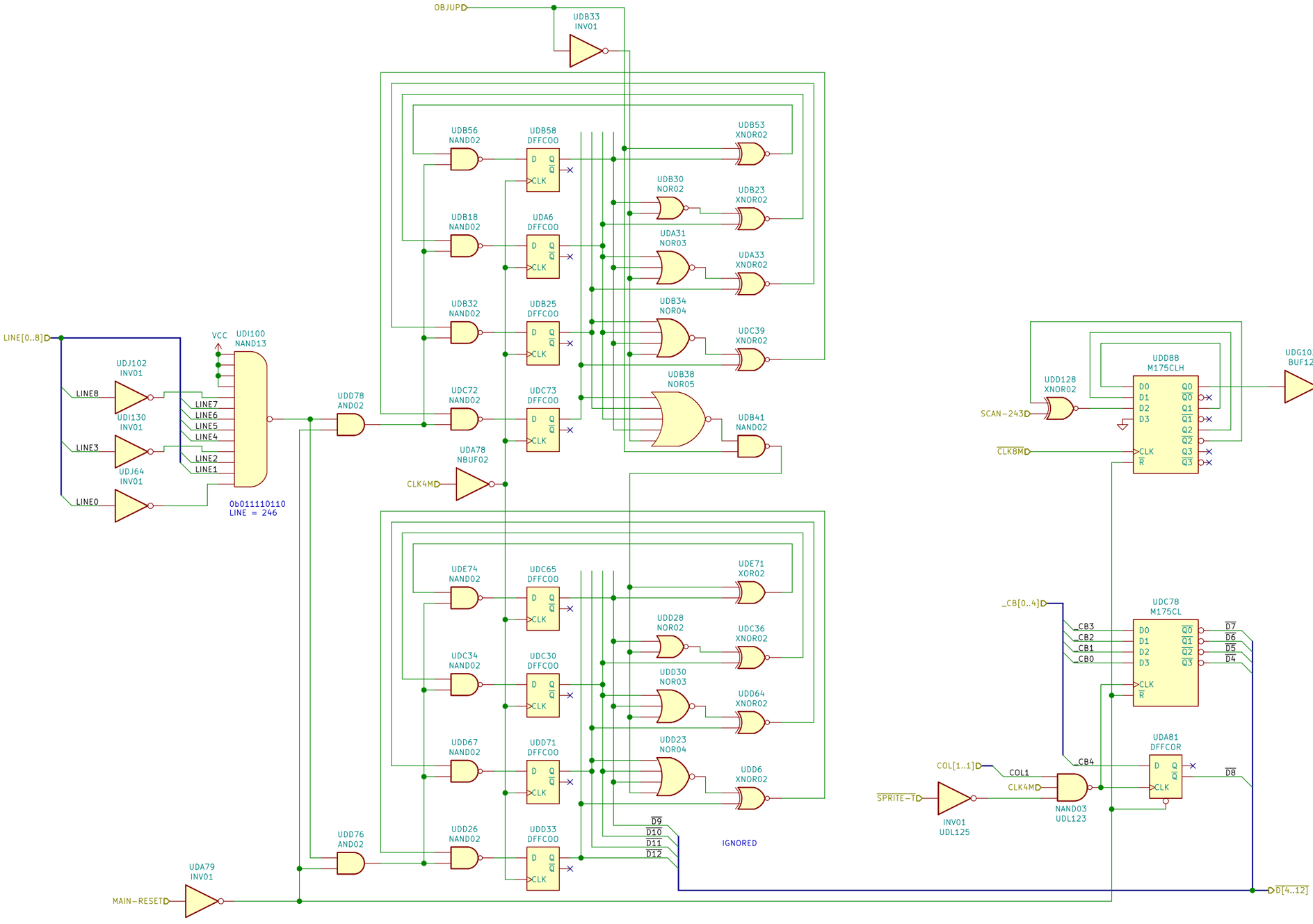

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Sheet: /vram-controller/vram-write-data/
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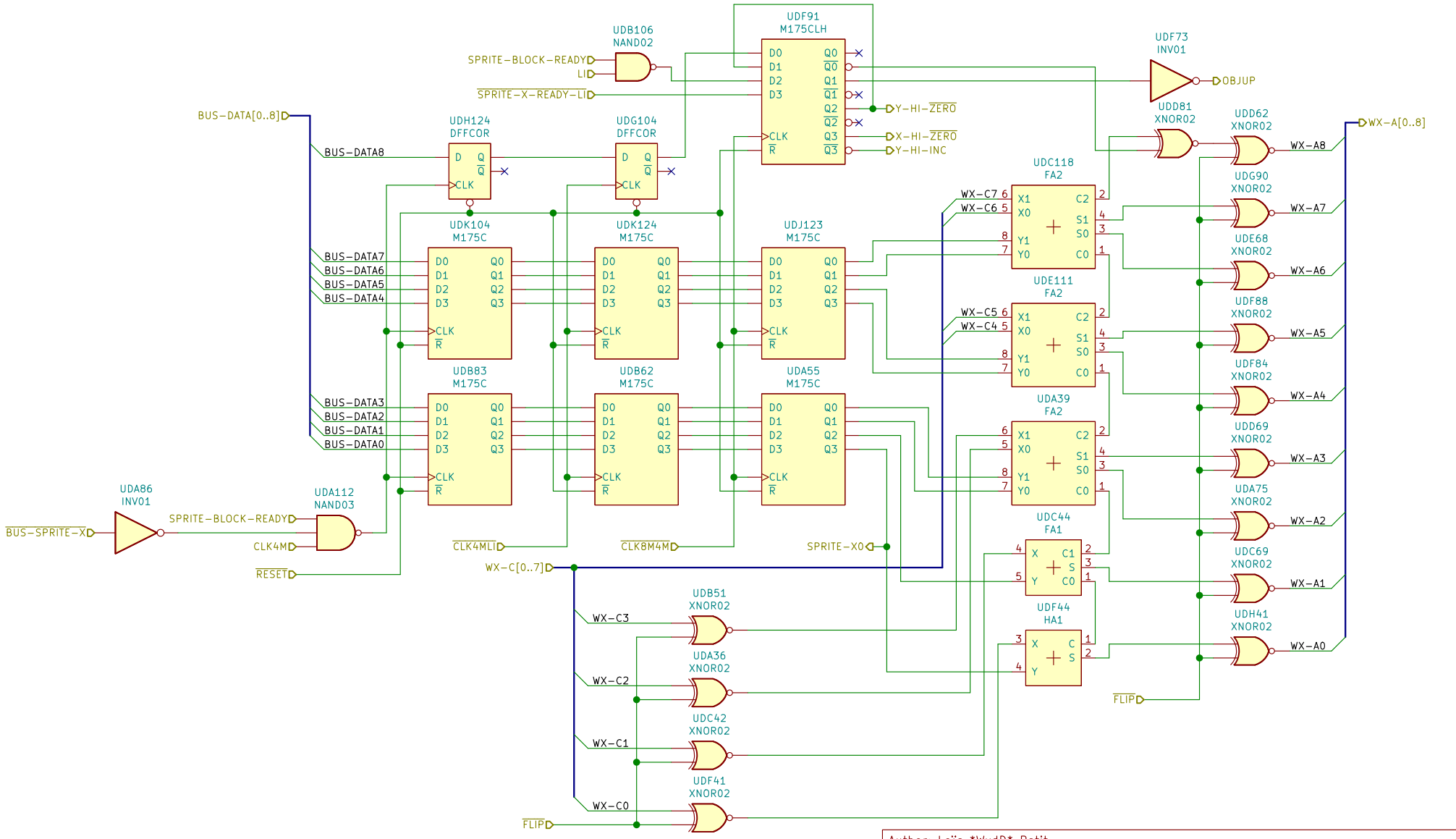
Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 34/83



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Sheet: /vram-controller/vram-write-x/
File: vram-write-x.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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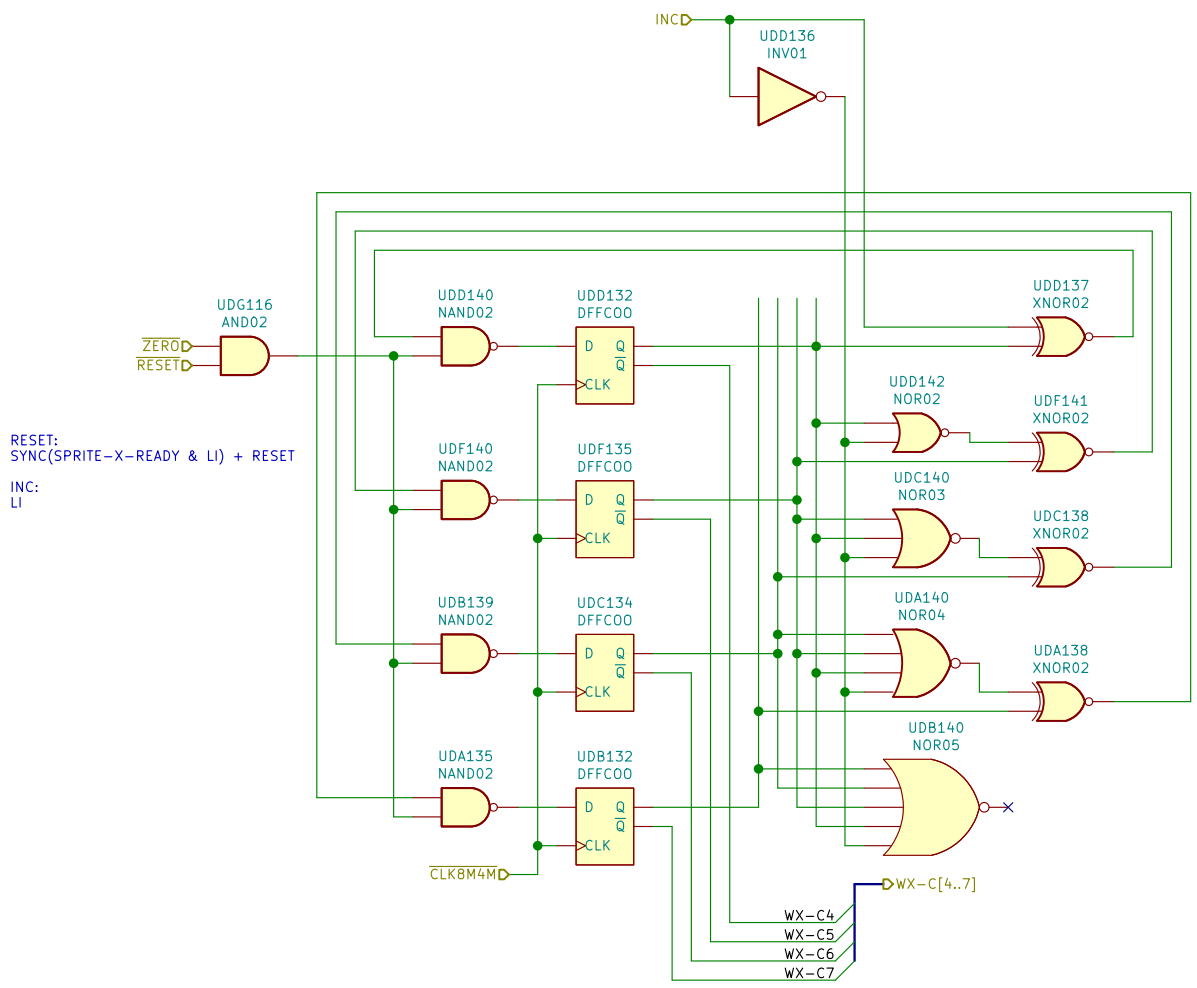

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Sheet: /vram-controller/vram-write-x-cnt-hi/
File: vram-write-x-cnt-hi.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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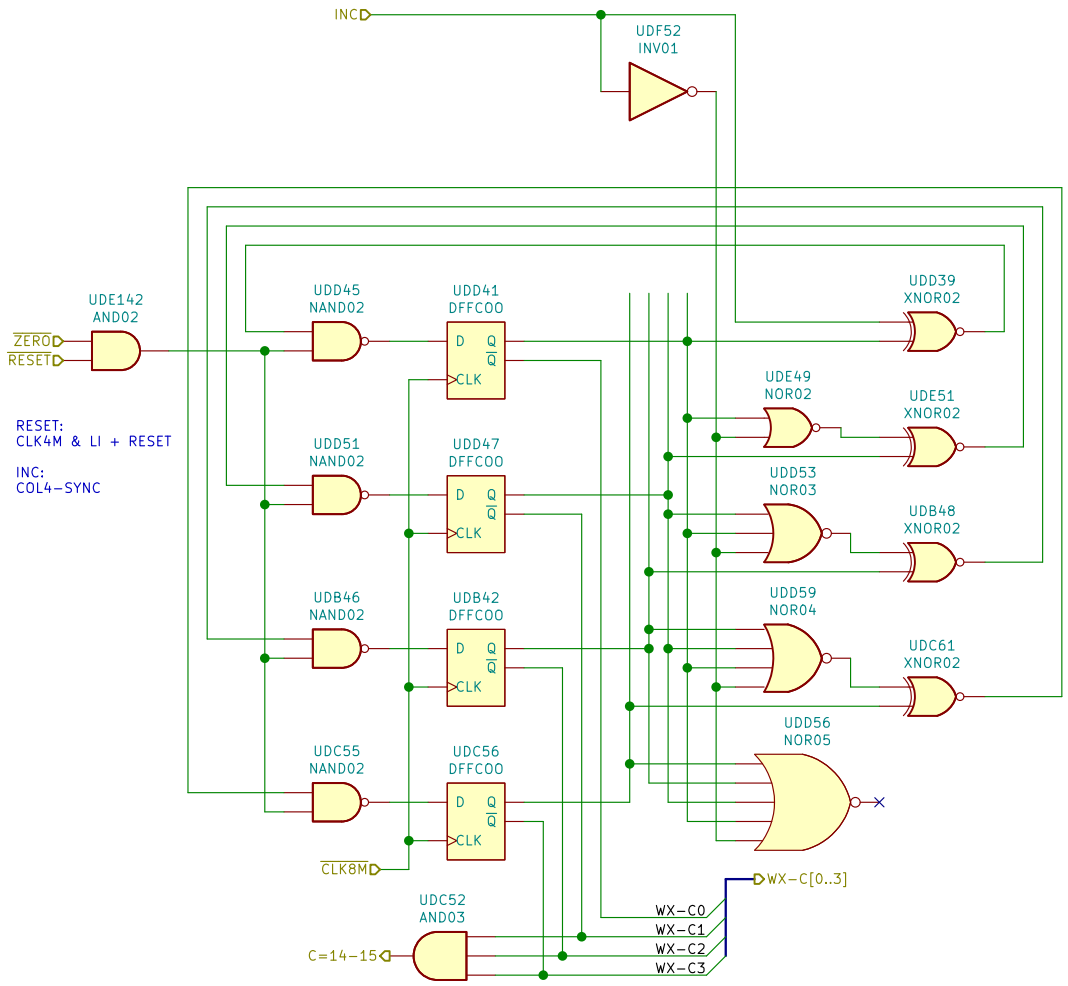

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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
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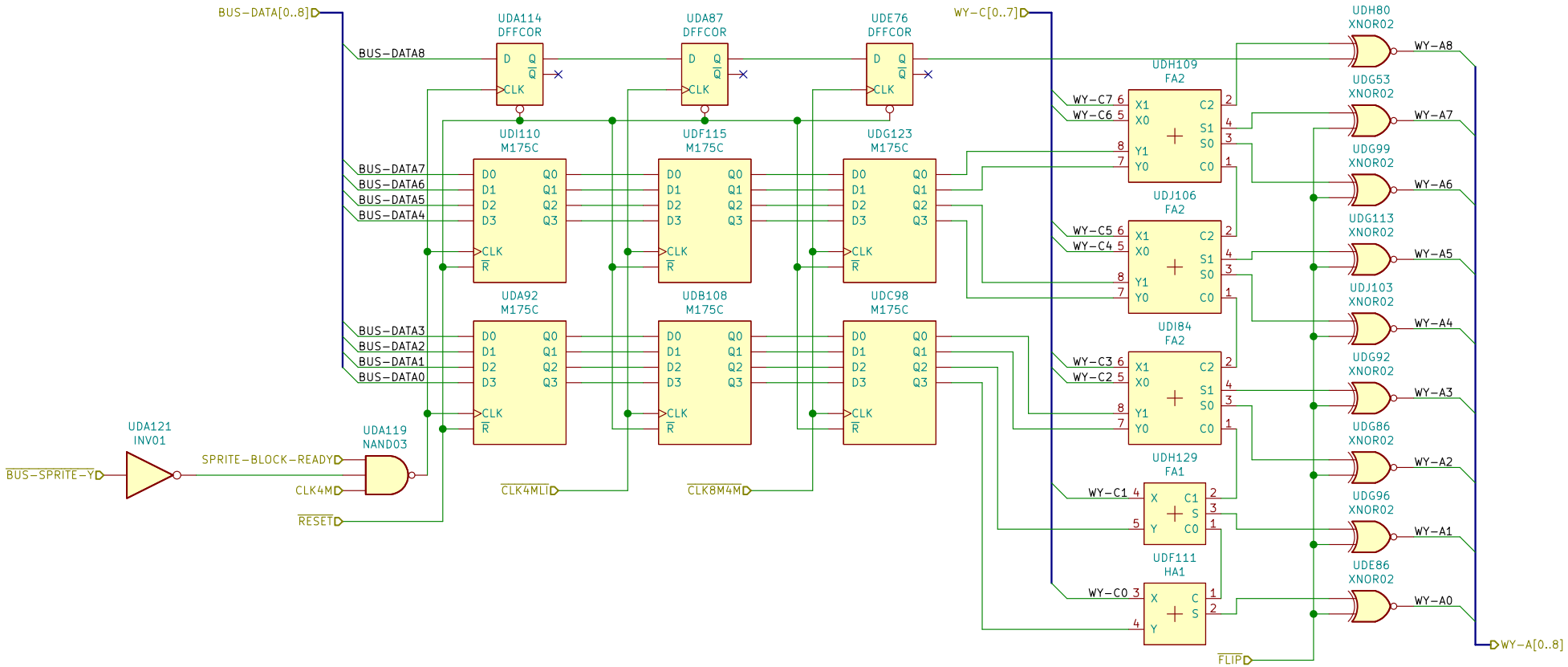

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Sheet: /vram-controller/vram-write-y/
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Title: CPS Reverse Engineering: DL-0311

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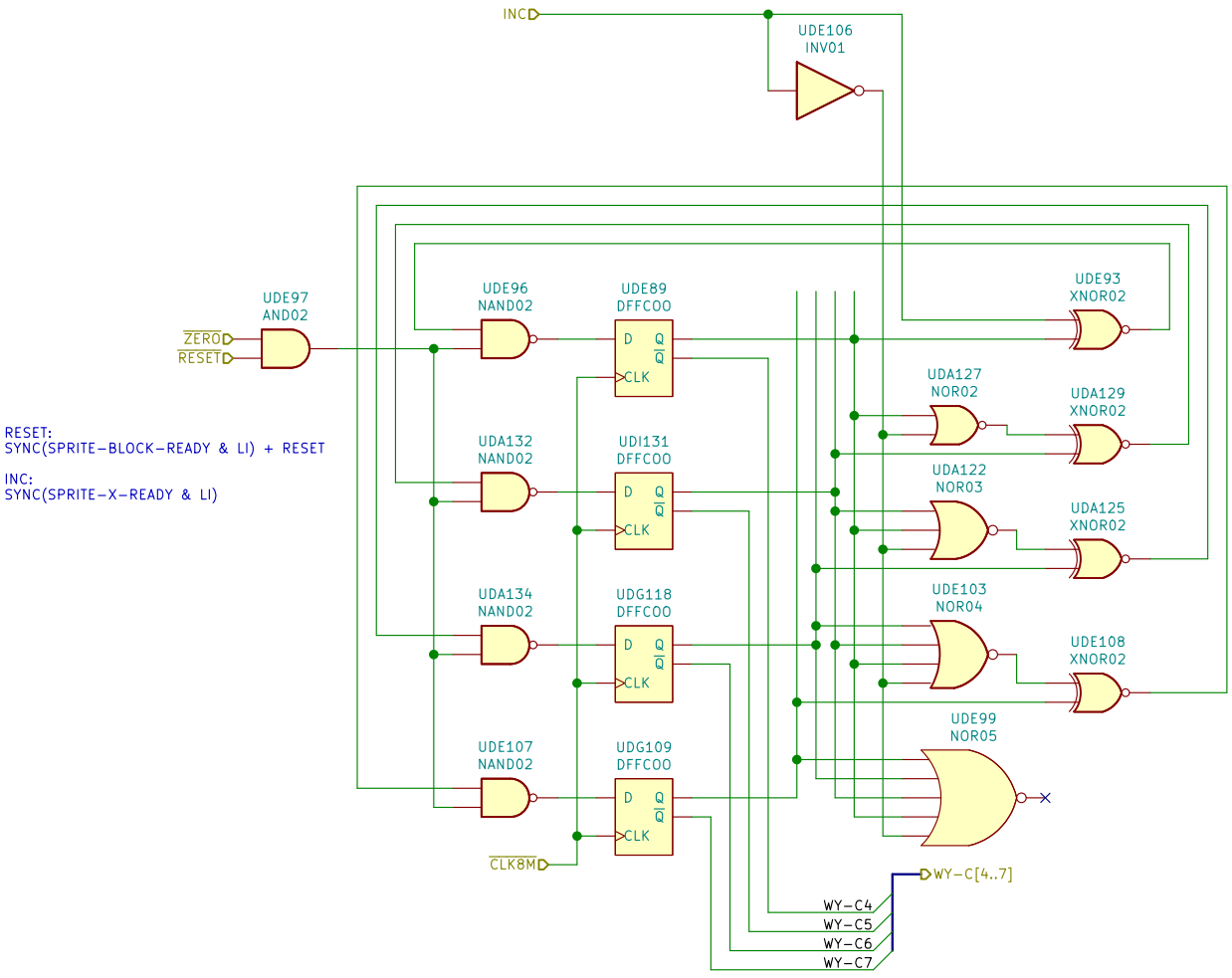

RESET:
SYNC(SPRITE-BLOCK-READY & LI) + RESET

INC:
SYNC(SPRITE-X-READY & LI)

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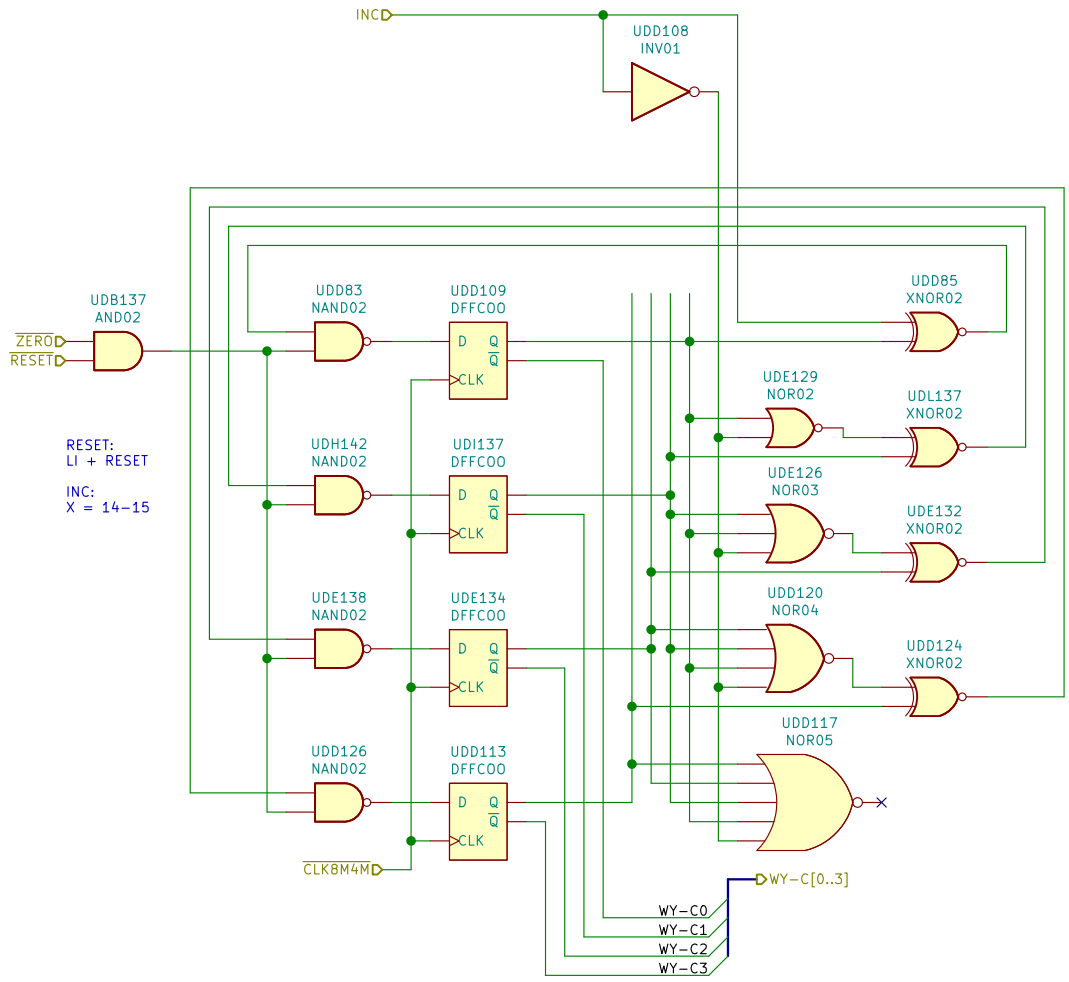
Sheet: /vram-controller/vram-write-y-cnt-hi/
File: vram-write-y-cnt-hi.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 39/83



Author: Loïc *WydD* Petit
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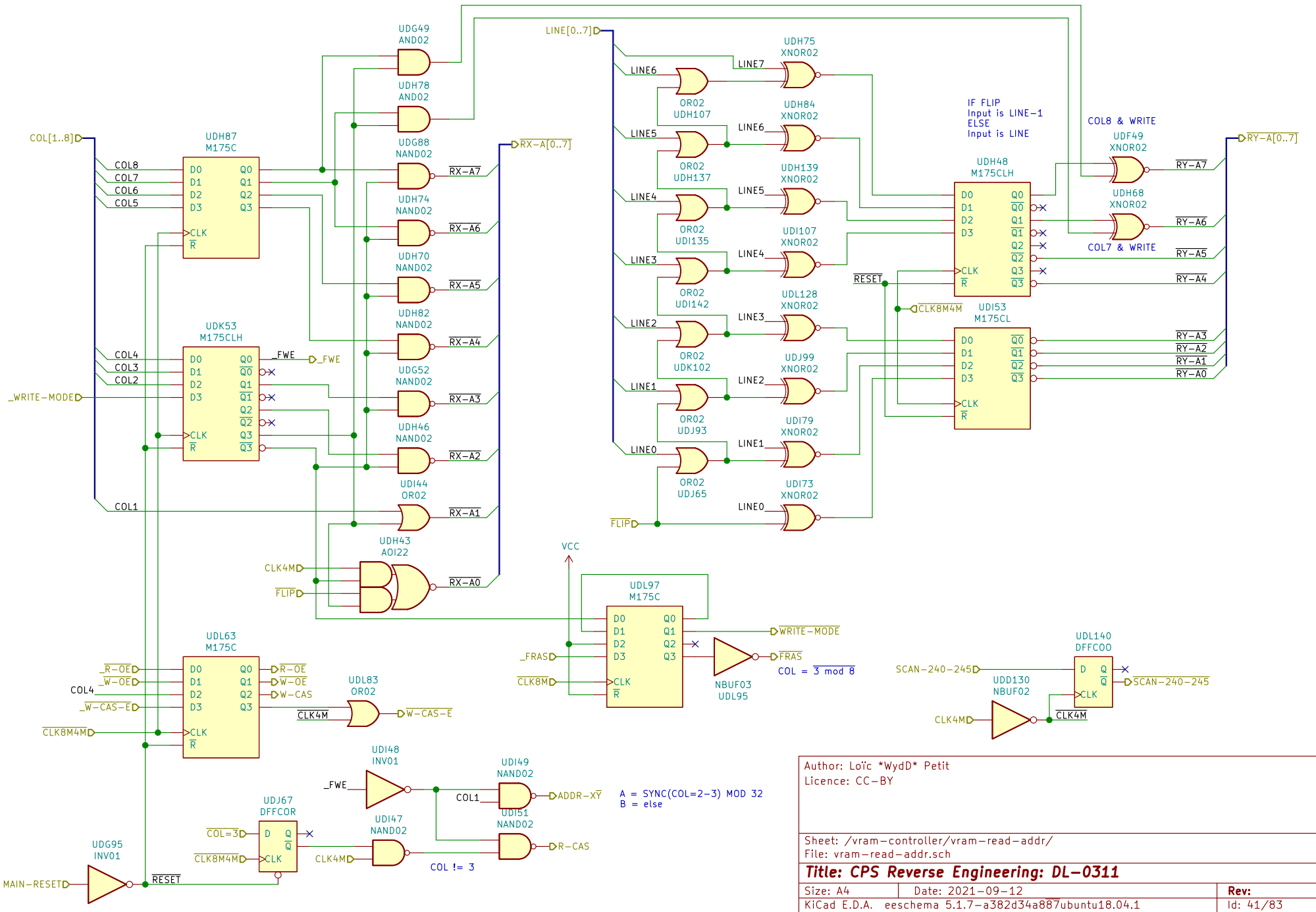
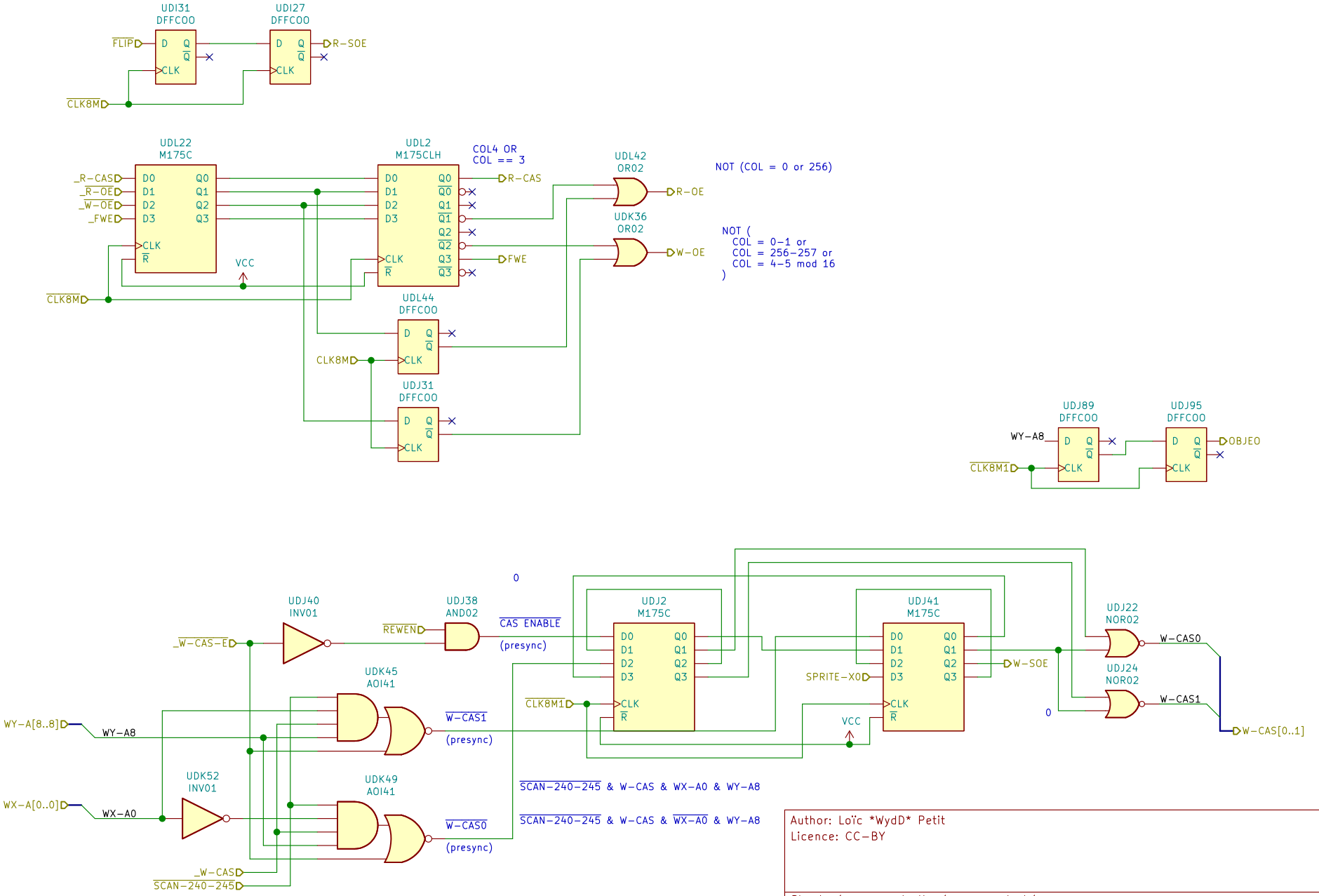
Sheet: /vram-controller/vram-write-y-cnt-lo/
File: vram-write-y-cnt-lo.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 40/83


UDG49 AND02
UDH78 AND02
UDG88 NAND02
UDH74 NAND02
UDH70 NAND02
UDH82 NAND02
UDG52 NAND02
UDH46 NAND02
UDI44 OR02
UDH43 AOI22
UDH87 M175C
UDK53 M175CLH
COL[1..8]
COL8
COL7
COL6
COL5
COL4
COL3
COL2
COL1
_WRITE-MODE
_FWE
CLK4M
FLIP
RX-A[0..7]
RX-A7
RX-A6
RX-A5
RX-A4
RX-A3
RX-A2
RX-A1
RX-A0
LINE[0..7]
UDH75 XNOR02
UDH84 XNOR02
UDH139 XNOR02
UDI107 XNOR02
UDL128 XNOR02
UDJ99 XNOR02
UDI79 XNOR02
UDI73 XNOR02
OR02 UDH107
OR02 UDH137
OR02 UDI135
OR02 UDI142
OR02 UDK102
OR02 UDJ93
OR02 UDJ65
LINE7
LINE6
LINE5
LINE4
LINE3
LINE2
LINE1
LINE0
IF FLIP
Input is LINE-1
ELSE
Input is LINE
UDH48 M175CLH
UDI53 M175CL
RESET
CLK8M4M
COL8 & WRITE
COL7 & WRITE
UDF49 XNOR02
UDH68 XNOR02
RY-A[0..7]
RY-A7
RY-A6
RY-A5
RY-A4
RY-A3
RY-A2
RY-A1
RY-A0
VCC
UDL97 M175C
_FRAS
CLK8M
WRITE-MODE
FRAS
NBUF03 UDL95
COL = 3 mod 8
UDL63 M175C
_R-OE
_W-OE
W-CAS
_W-CAS-E
CLK8M4M
UDL83 OR02
W-CAS-E
UDL140 DFFCOO
UDD130 NBUF02
SCAN-240-245
UDI48 INV01
UDI49 NAND02
UDI51 NAND02
UDI47 NAND02
UDJ67 DFFCOR
UDG95 INV01
MAIN-RESET
ADDR-XY
R-CAS
A = SYNC(COL=2-3) MOD 32
B = else
COL != 3
Author: Loïc *WydD* Petit
Licence: CC-BY
Sheet: /vram-controller/vram-read-addr/
File: vram-read-addr.sch
Title: CPS Reverse Engineering: DL-0311
Size: A4
Date: 2021-09-12
Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1
Id: 41/83



Author: Loïc *WydD* Petit
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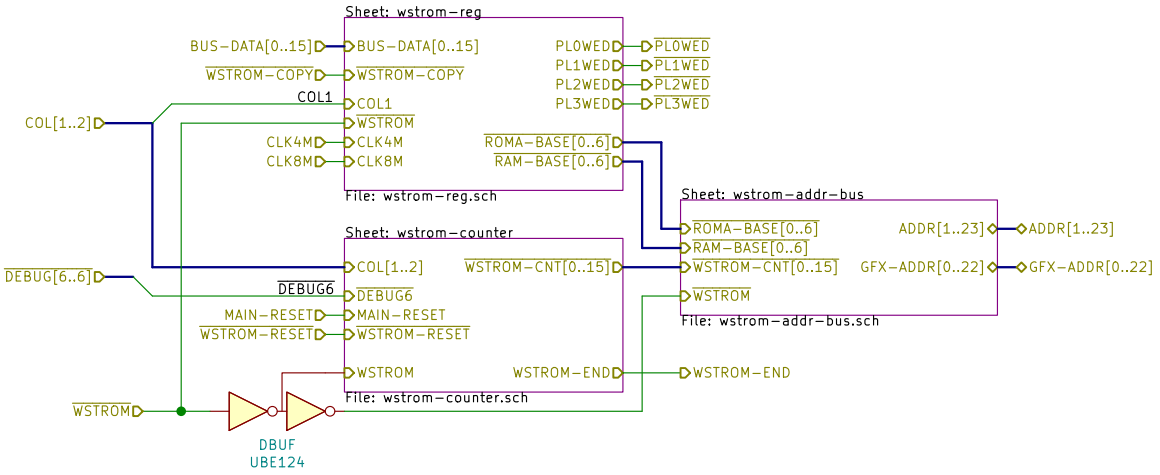
Sheet: /vram-controller/vram-control/
File: vram-control.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 42/83



Author: Loïc *WydD* Petit
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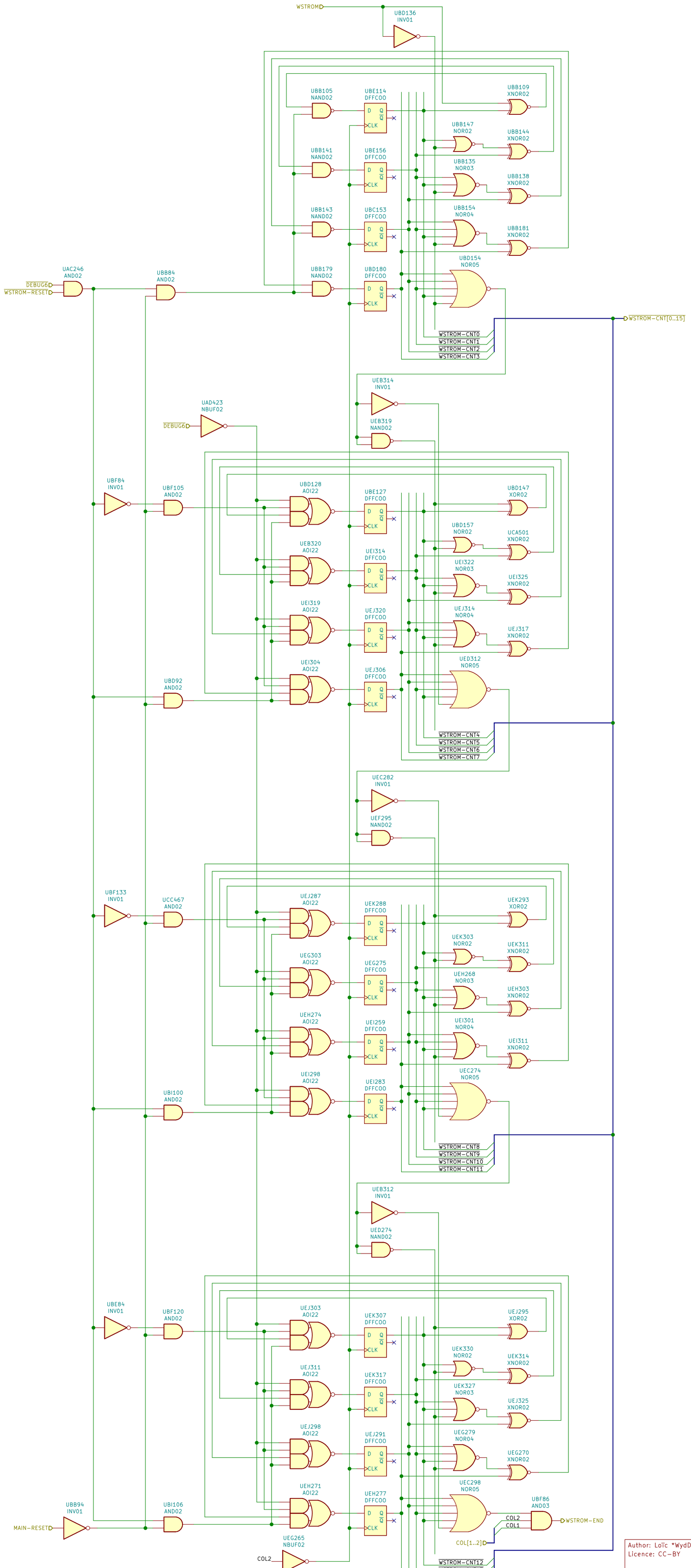
Sheet: /wstrom/
File: wstrom.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 43/83



Author: Loïc *WydD* Petit
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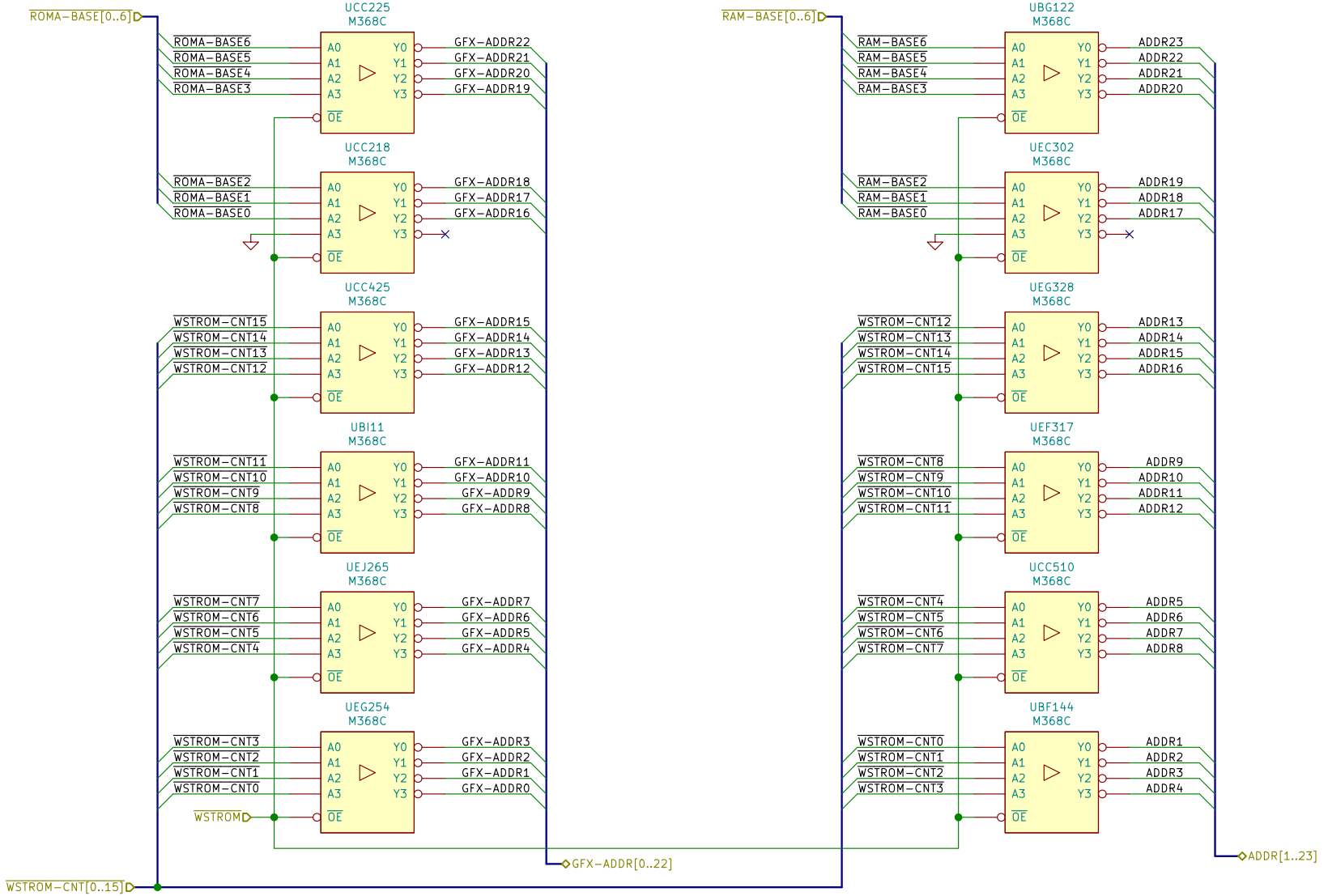
Sheet: /wstrom/wstrom-counter/
File: wstrom-counter.sch

Title: CPS Reverse Engineering: DL-0311

Size: A2	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 44/83

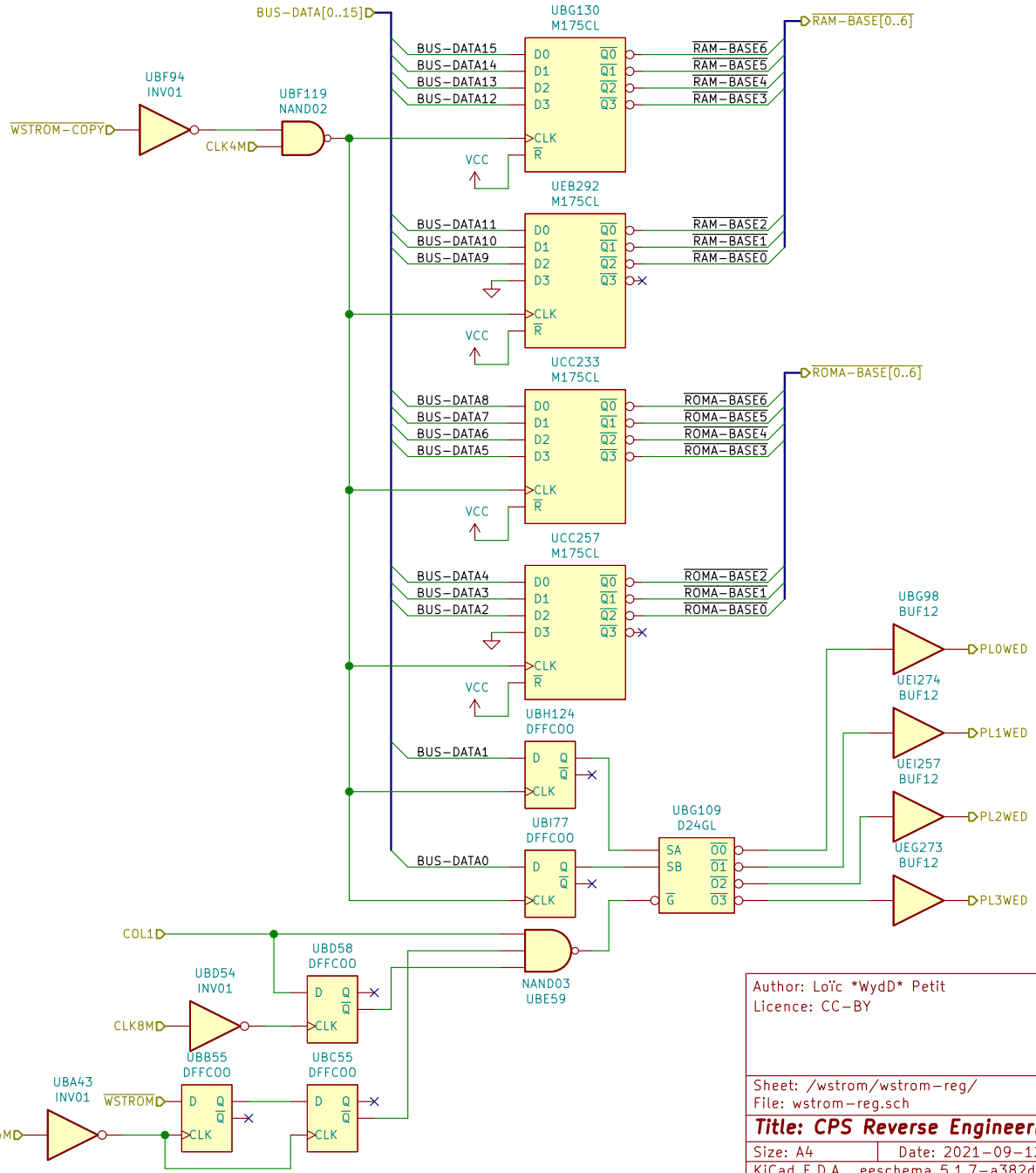


Author: Loïc *WydD* Petit
Licence: CC-BY

Sheet: /wstrom/wstrom-addr-bus/
File: wstrom-addr-bus.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 45/83



Author: Loïc *WydD* Petit
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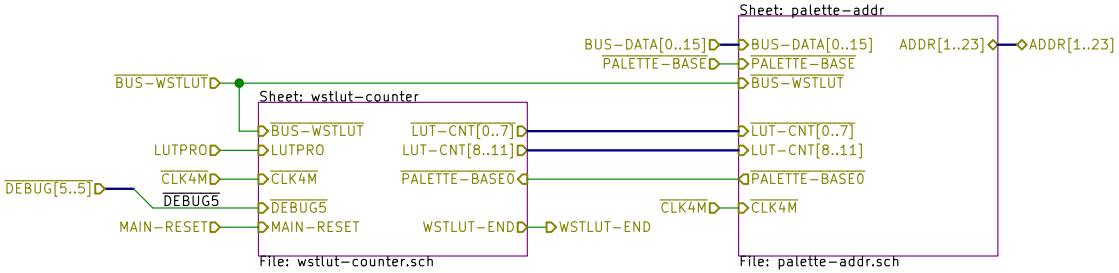
Sheet: /wstrom/wstrom-reg/
File: wstrom-reg.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 46/83



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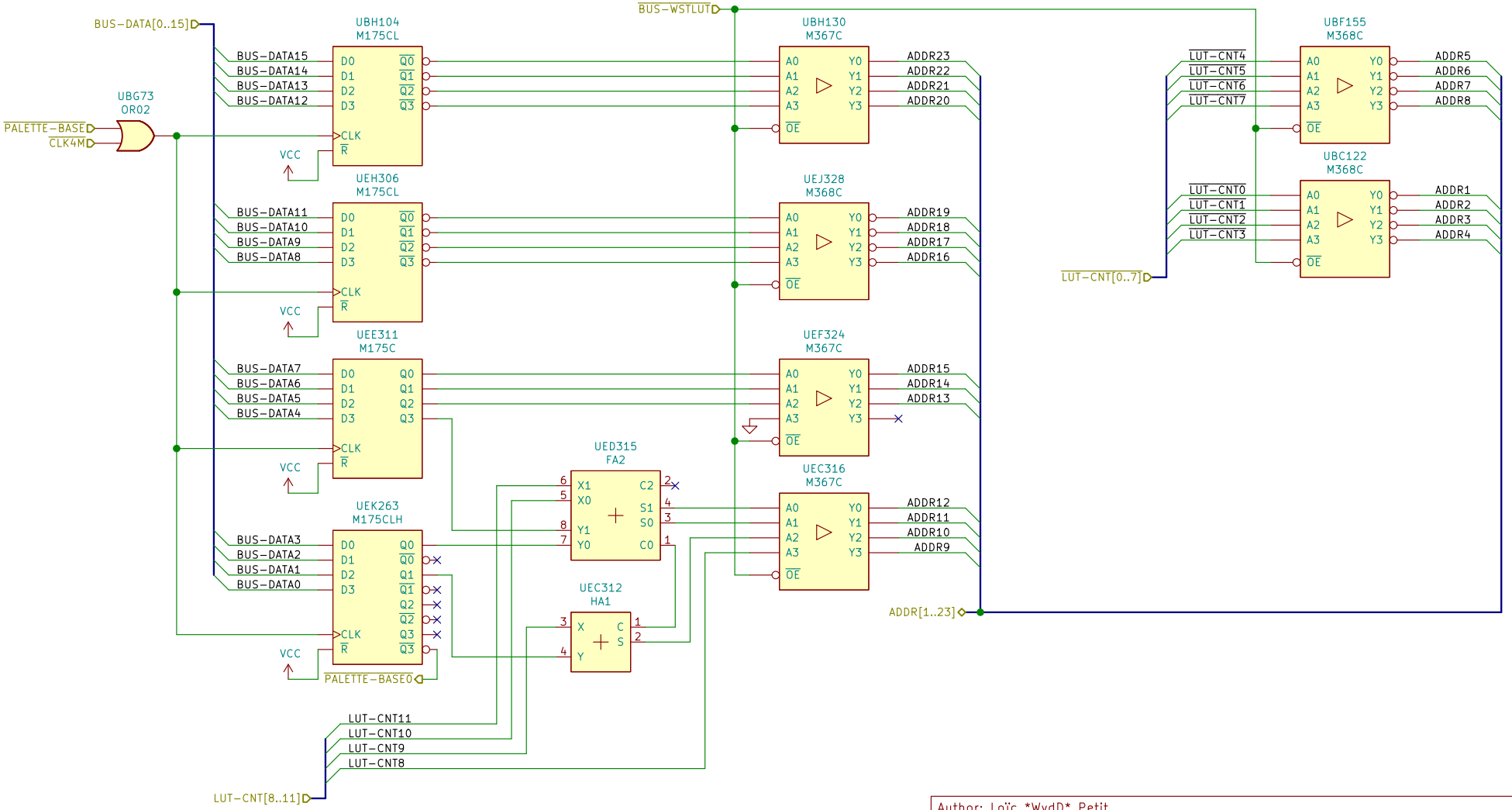
Sheet: /wstlut/
File: wstlut.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 47/83



Author: Loïc *WydD* Petit
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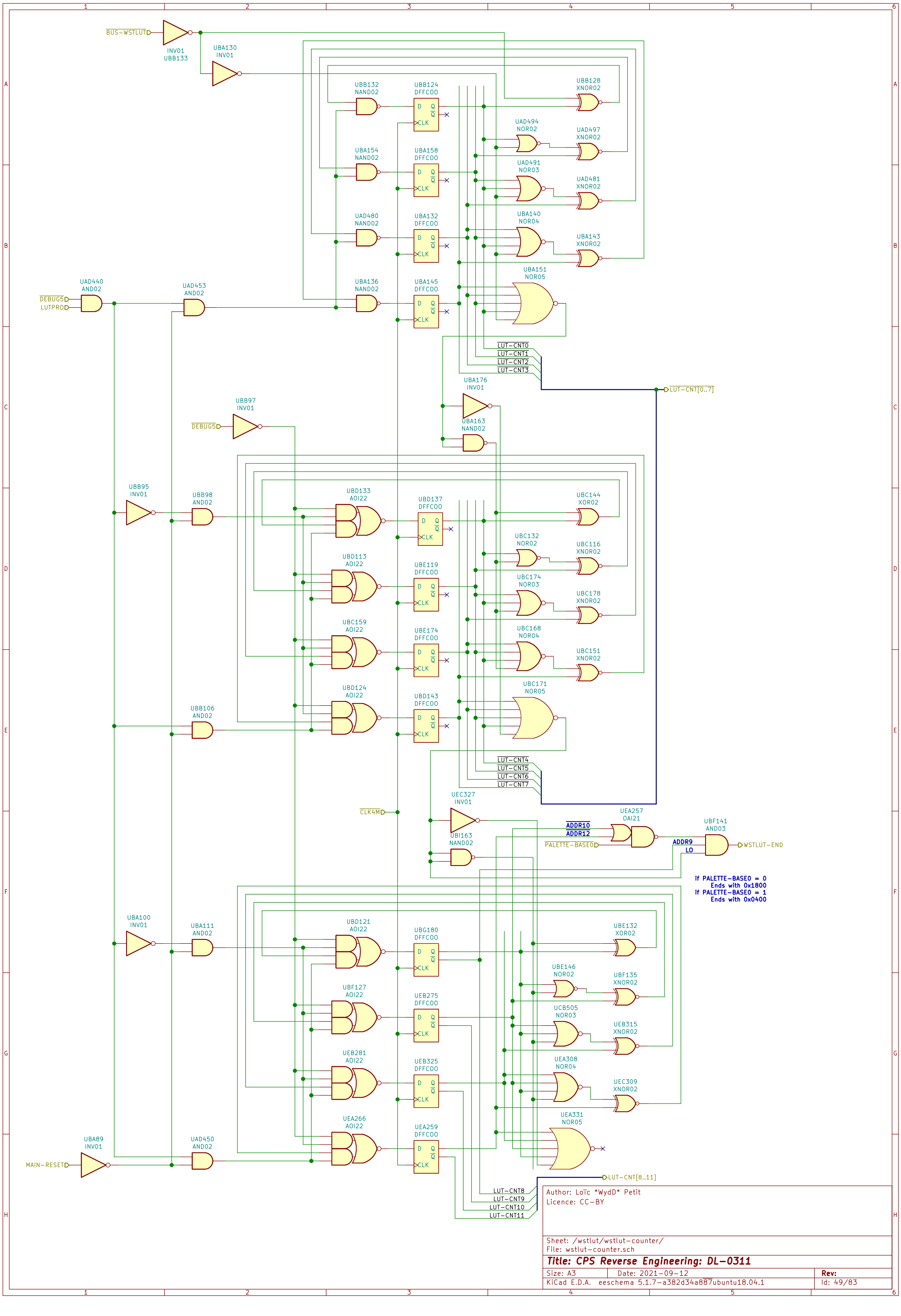
Sheet: /wstlut/palette-addr/
File: palette-addr.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 48/83


BUS-WSTLUT
INV01
UBB133
UBA130
INV01
UBB132
NAND02
UBB124
DFFC00
UBB128
XNOR02
UAD494
NOR02
UAD497
XNOR02
UBA154
NAND02
UBA158
DFFC00
UAD491
NOR03
UAD481
XNOR02
UAD480
NAND02
UBA132
DFFC00
UBA140
NOR04
UBA143
XNOR02
UBA151
NOR05
UAD440
AND02
DEBUG5
LUTPRO
UAD453
AND02
UBA136
NAND02
UBA145
DFFC00
LUT-CNT0
LUT-CNT1
LUT-CNT2
LUT-CNT3
UBA176
INV01
LUT-CNT[0..7]
UBB97
INV01
DEBUG5
UBA163
NAND02
UBB95
INV01
UBB98
AND02
UBD133
AOI22
UBD137
DFFC00
UBC144
XOR02
UBC132
NOR02
UBC116
XNOR02
UBD113
AOI22
UBE119
DFFC00
UBC174
NOR03
UBC178
XNOR02
UBC159
AOI22
UBE174
DFFC00
UBC168
NOR04
UBC151
XNOR02
UBD124
AOI22
UBD143
DFFC00
UBC171
NOR05
UBB106
AND02
LUT-CNT4
LUT-CNT5
LUT-CNT6
LUT-CNT7
UEC327
INV01
CLK4M
UEA257
OAI21
UBF141
AND03
ADDR10
ADDR12
PALETTE-BASE0
ADDR9
LO
WSTLUT-END
UBI163
NAND02
If PALETTE-BASE0 = 0
Ends with 0x1800
If PALETTE-BASE0 = 1
Ends with 0x0400
UBA100
INV01
UBA111
AND02
UBD121
AOI22
UBG180
DFFC00
UBE132
XOR02
UBE146
NOR02
UBF135
XNOR02
UBF127
AOI22
UEB275
DFFC00
UCB505
NOR03
UEB315
XNOR02
UEB281
AOI22
UEB325
DFFC00
UEA308
NOR04
UEC309
XNOR02
UEA266
AOI22
UEA259
DFFC00
UEA331
NOR05
UBA89
INV01
MAIN-RESET
UAD450
AND02
LUT-CNT[8..11]
LUT-CNT8
LUT-CNT9
LUT-CNT10
LUT-CNT11
Author: Loïc *WydD* Petit
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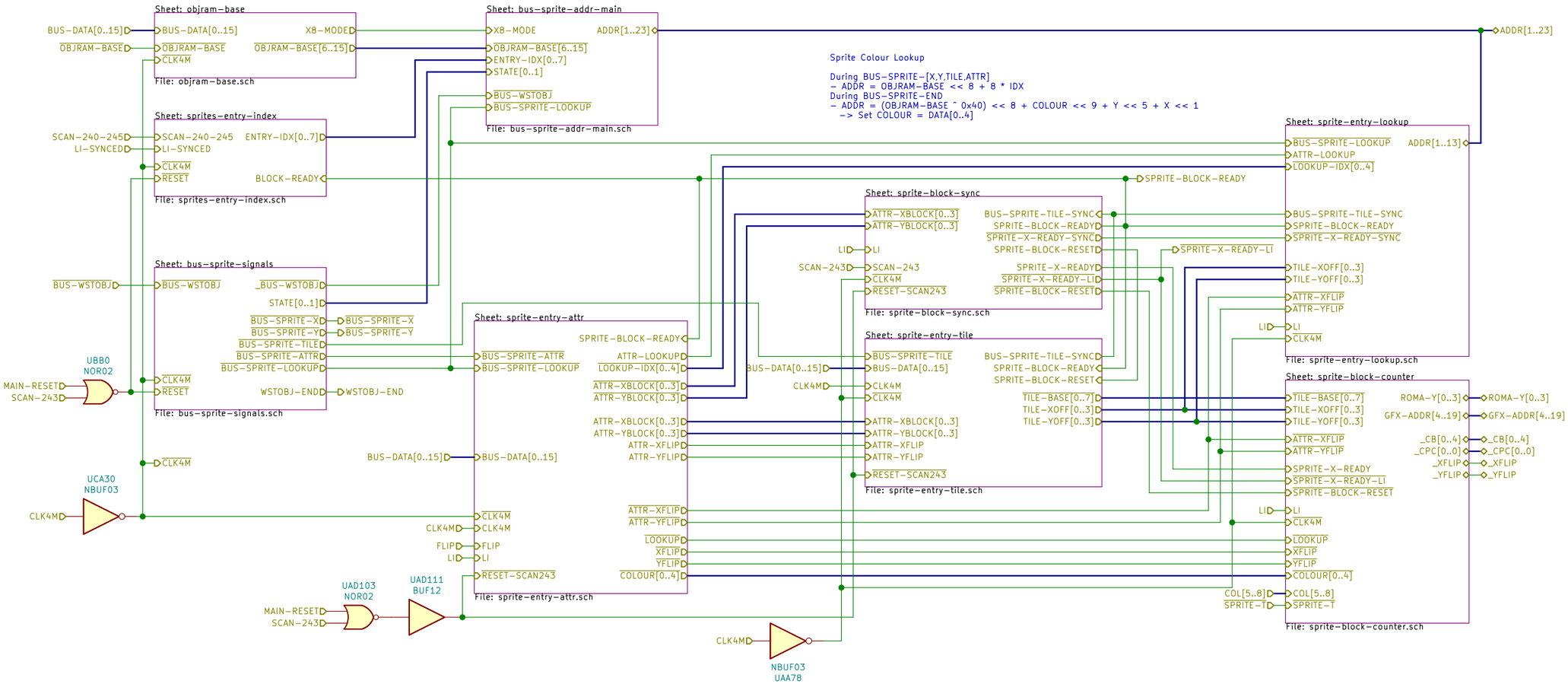
Sheet: /wstlut/wstlut-counter/
File: wstlut-counter.sch
Title: CPS Reverse Engineering: DL-0311
Size: A3
Date: 2021-09-12
Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1
Id: 49/83



Author: Loïc *WydD* Petit
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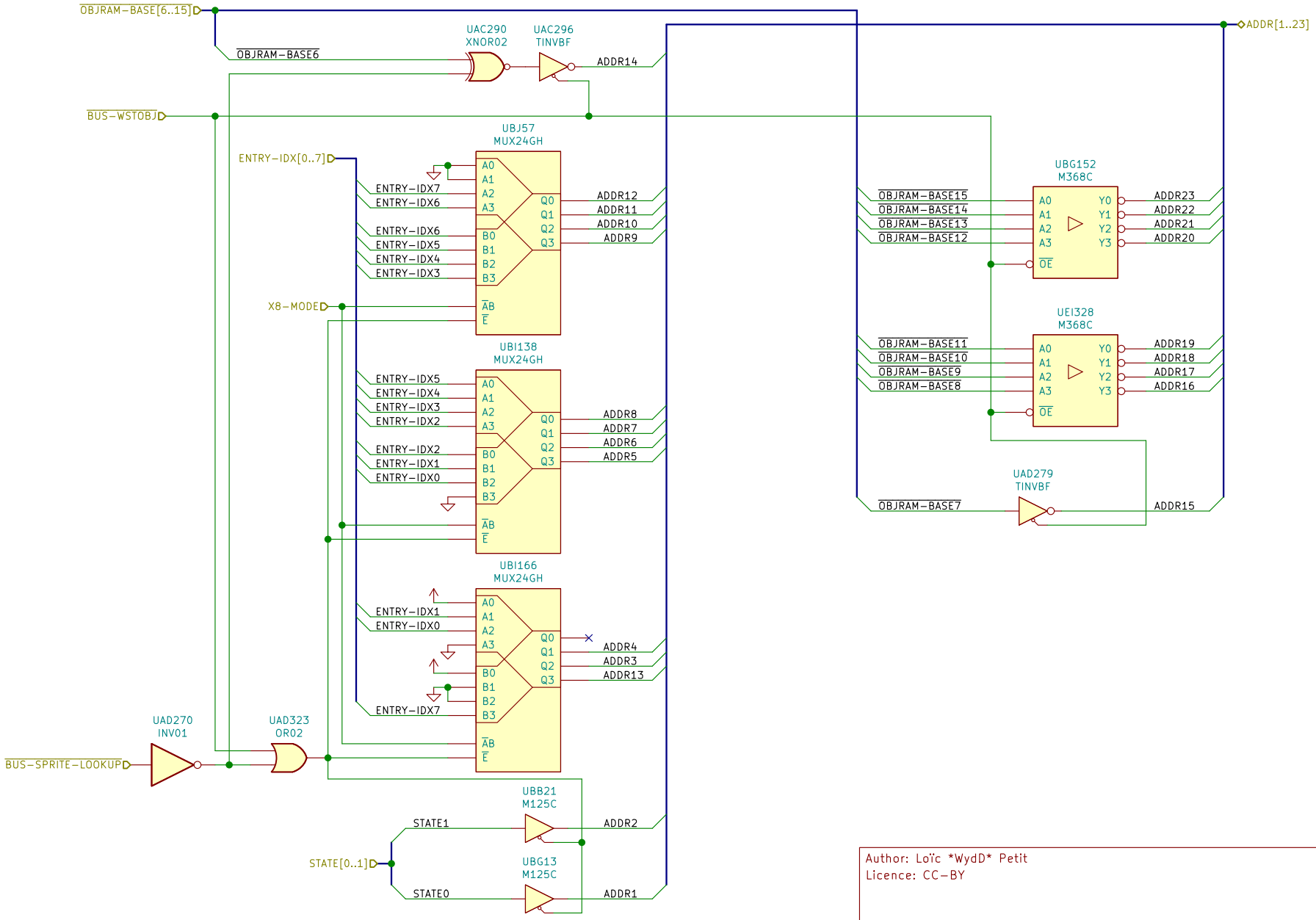
Sheet: /sprites-controller/
File: sprites-controller.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 50/83



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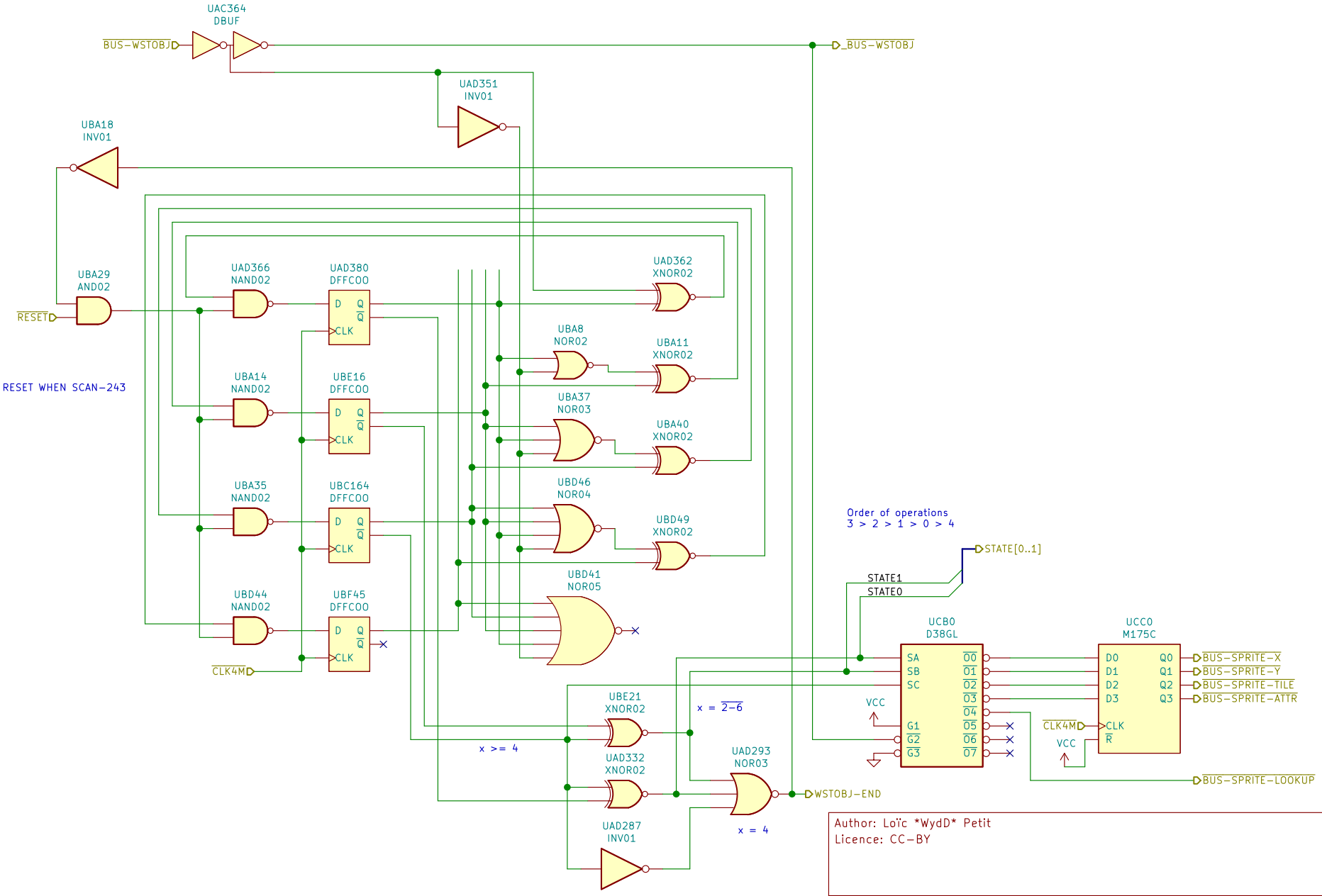
Sheet: /sprites-controller/bus-sprite-addr-main/
File: bus-sprite-addr-main.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 51/83



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Sheet: /sprites-controller/bus-sprite-signals/
File: bus-sprite-signals.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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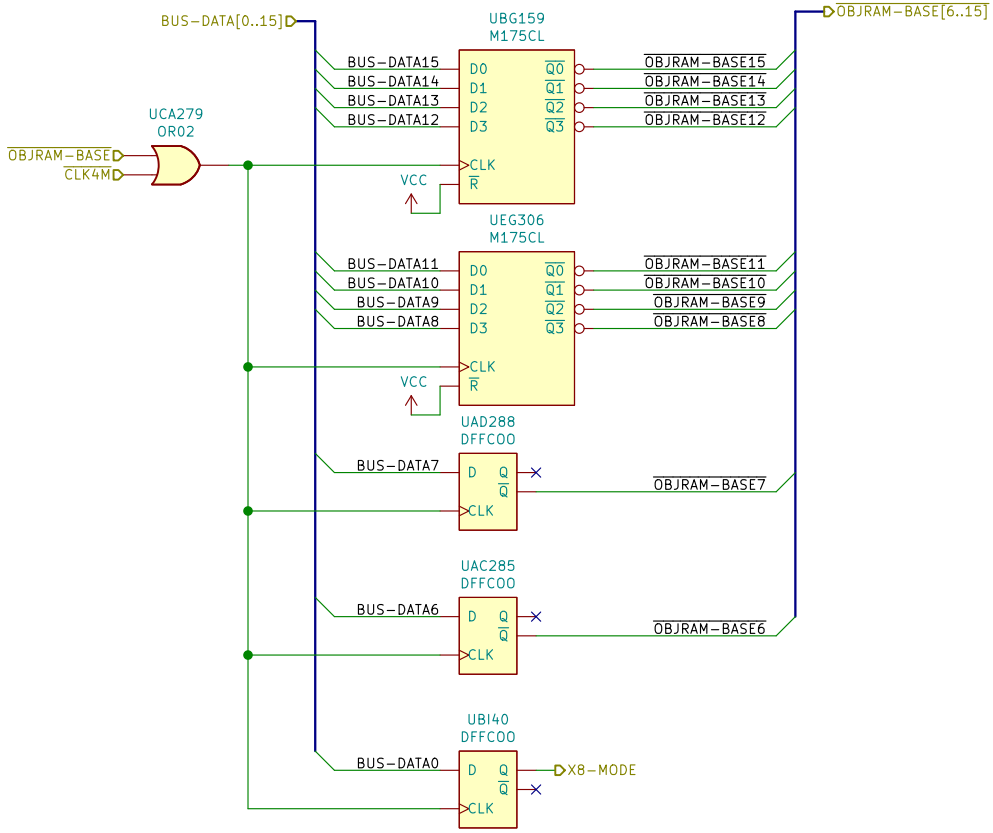

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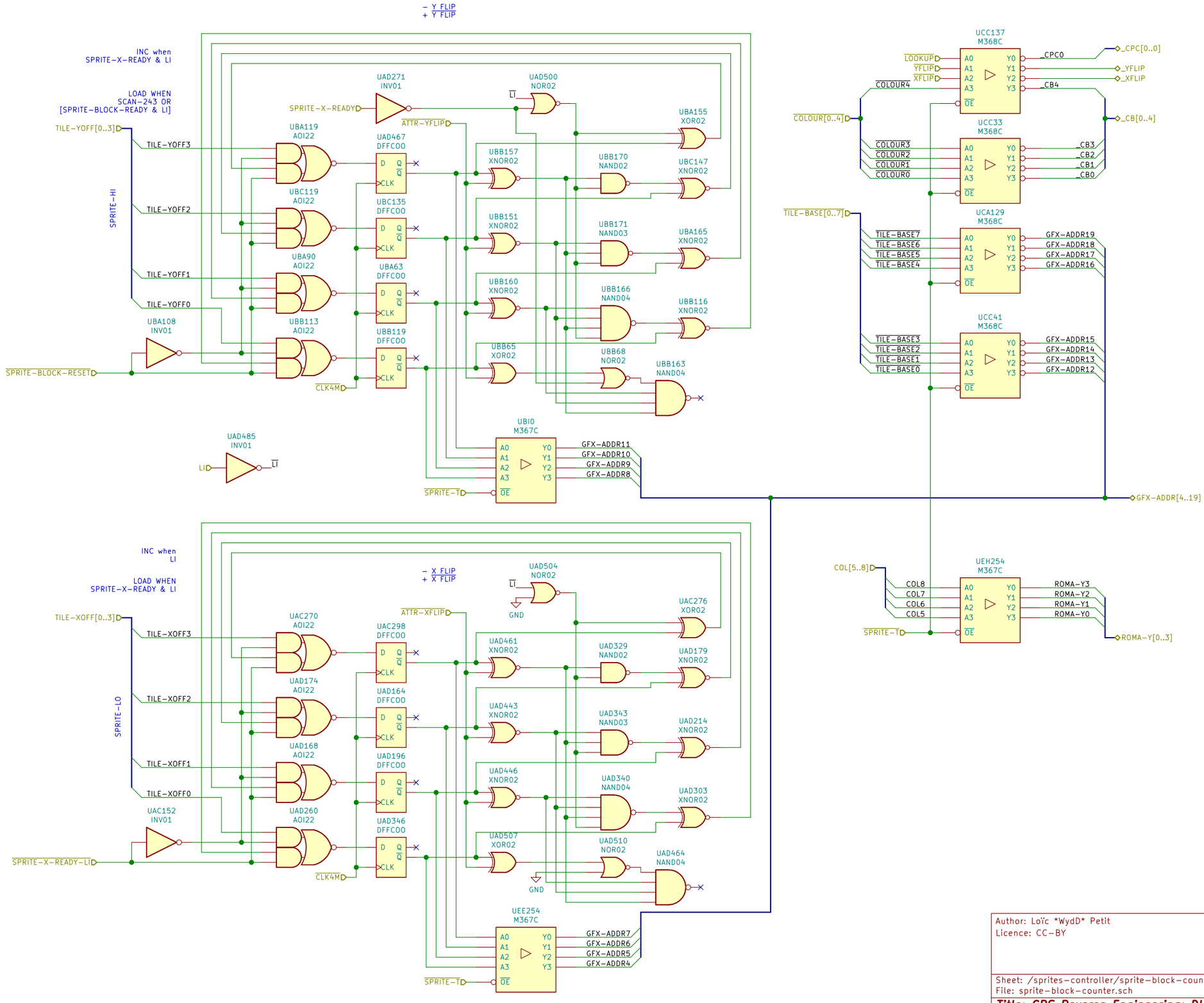
Sheet: /sprites-controller/objram-base/
File: objram-base.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 53/83



Author: Loïc *WydD* Petit
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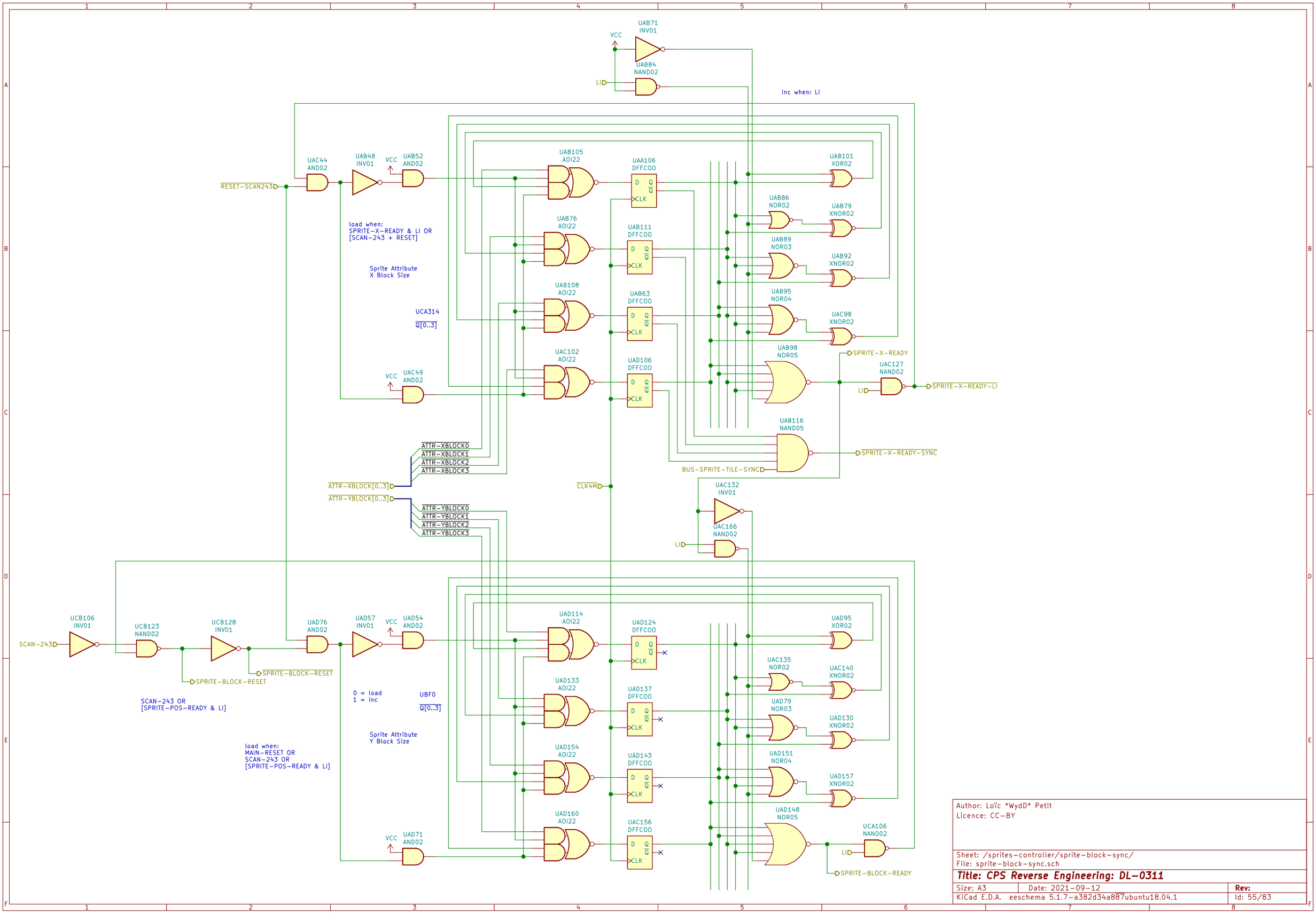
Sheet: /sprites-controller/sprite-block-counter/
File: sprite-block-counter.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 54/83



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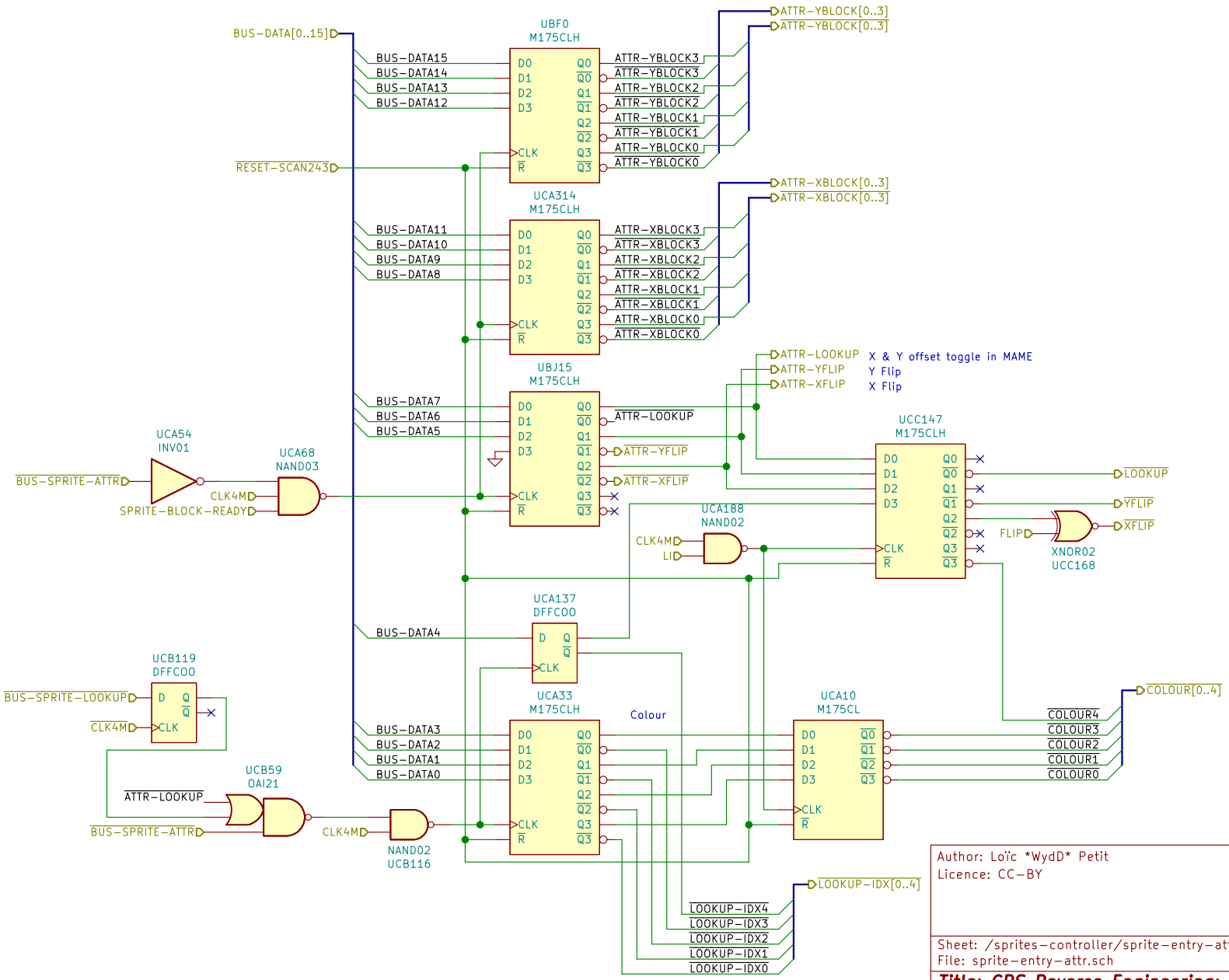
Sheet: /sprites-controller/sprite-block-sync/
File: sprite-block-sync.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 55/83



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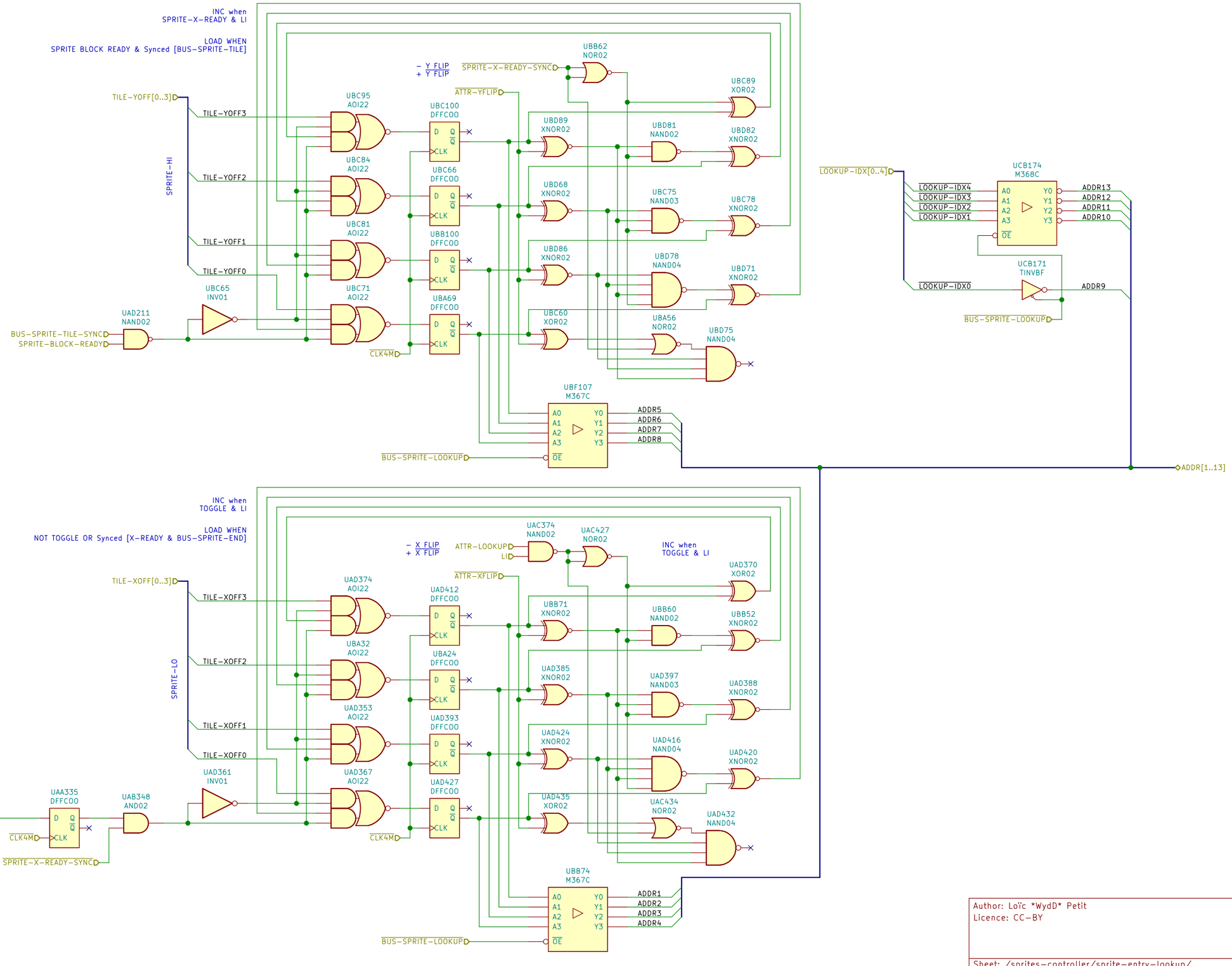
Sheet: /sprites-controller/sprite-entry-attr/
File: sprite-entry-attr.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 56/83



Author: Loïc *WydD* Petit
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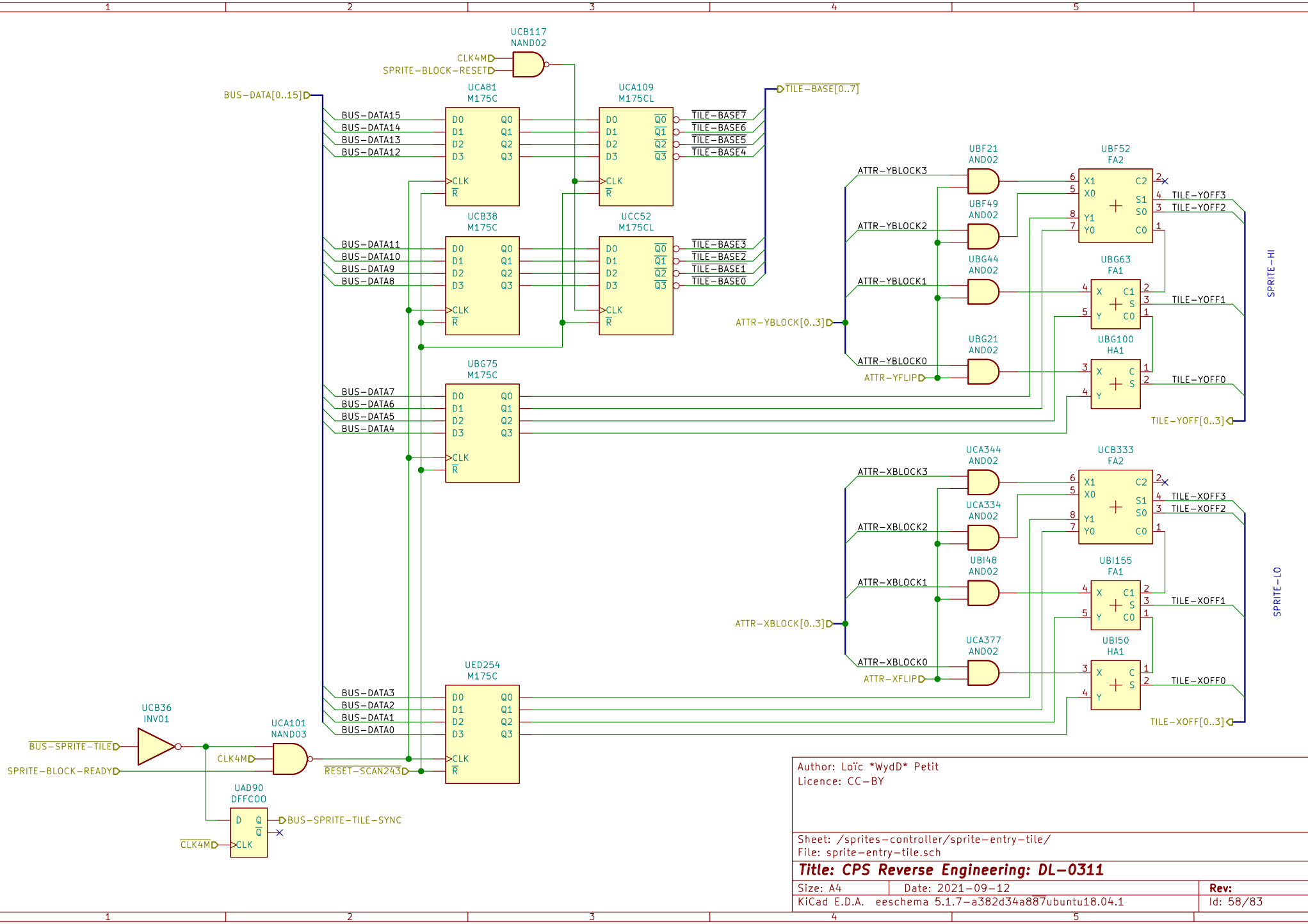
Sheet: /sprites-controller/sprite-entry-lookup/
File: sprite-entry-lookup.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 57/83


UCB117
NAND02
CLK4M
SPRITE-BLOCK-RESET
BUS-DATA[0..15]
UCA81
M175C
UCA109
M175CL
TILE-BASE[0..7]
BUS-DATA15
BUS-DATA14
BUS-DATA13
BUS-DATA12
TILE-BASE7
TILE-BASE6
TILE-BASE5
TILE-BASE4
UCB38
M175C
UCC52
M175CL
BUS-DATA11
BUS-DATA10
BUS-DATA9
BUS-DATA8
TILE-BASE3
TILE-BASE2
TILE-BASE1
TILE-BASE0
UBG75
M175C
BUS-DATA7
BUS-DATA6
BUS-DATA5
BUS-DATA4
UED254
M175C
BUS-DATA3
BUS-DATA2
BUS-DATA1
BUS-DATA0
UBF21
AND02
UBF49
AND02
UBG44
AND02
UBG21
AND02
ATTR-YBLOCK3
ATTR-YBLOCK2
ATTR-YBLOCK1
ATTR-YBLOCK0
ATTR-YBLOCK[0..3]
ATTR-YFLIP
UBF52
FA2
UBG63
FA1
UBG100
HA1
TILE-YOFF3
TILE-YOFF2
TILE-YOFF1
TILE-YOFF0
TILE-YOFF[0..3]
SPRITE-HI
UCA344
AND02
UCA334
AND02
UBI48
AND02
UCA377
AND02
ATTR-XBLOCK3
ATTR-XBLOCK2
ATTR-XBLOCK1
ATTR-XBLOCK0
ATTR-XBLOCK[0..3]
ATTR-XFLIP
UCB333
FA2
UBI155
FA1
UBI150
HA1
TILE-XOFF3
TILE-XOFF2
TILE-XOFF1
TILE-XOFF0
TILE-XOFF[0..3]
SPRITE-LO
UCB36
INV01
UCA101
NAND03
BUS-SPRITE-TILE
SPRITE-BLOCK-READY
CLK4M
RESET-SCAN243
UAD90
DFFCOO
BUS-SPRITE-TILE-SYNC
CLK4M
Author: Loïc *WydD* Petit
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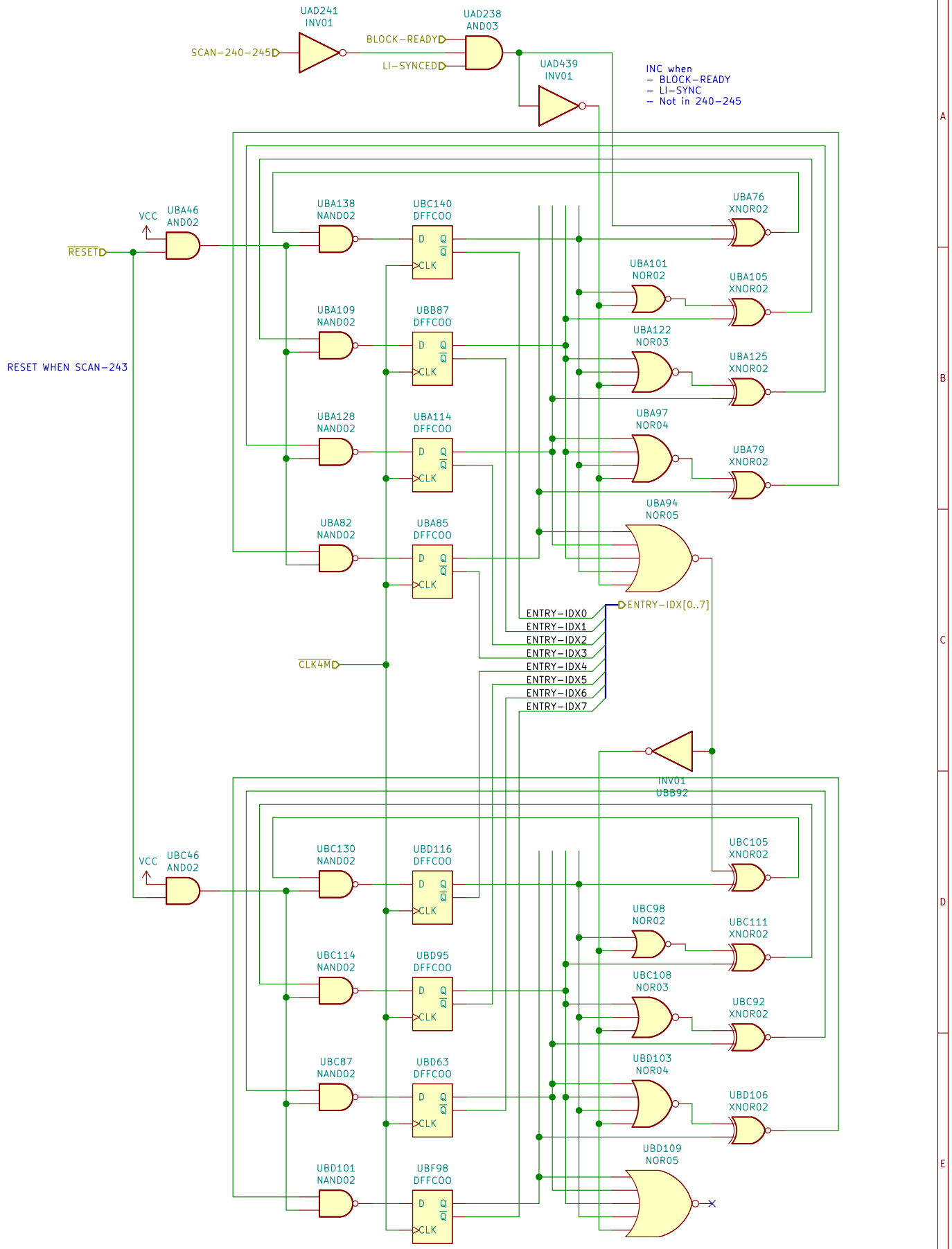
Sheet: /sprites-controller/sprite-entry-tile/
File: sprite-entry-tile.sch
Title: CPS Reverse Engineering: DL-0311
Size: A4
Date: 2021-09-12
Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1
Id: 58/83



Author: Loïc *WydD* Petit
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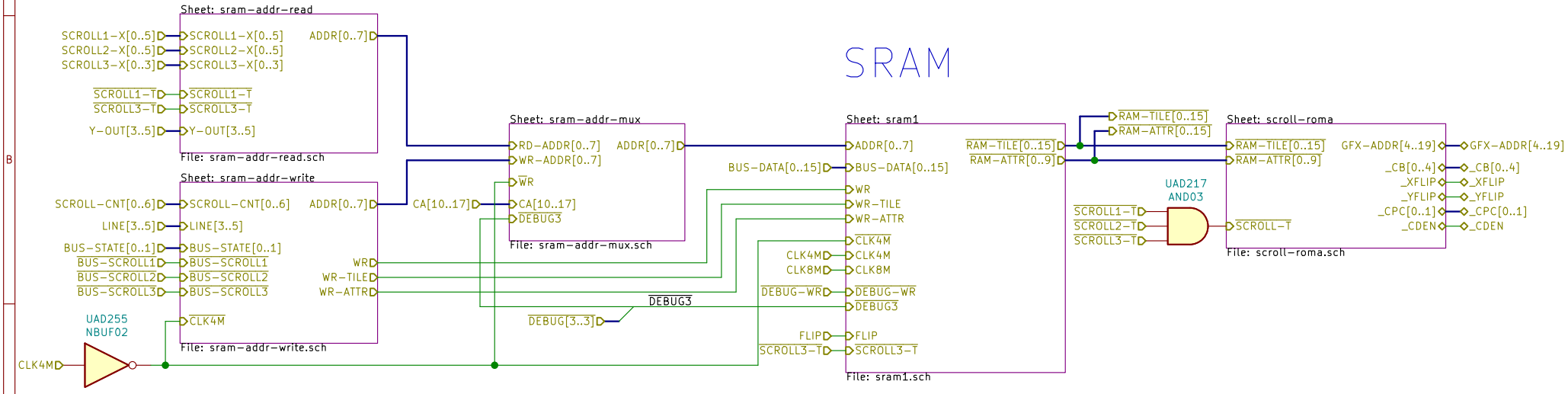
Sheet: /sprites-controller/sprites-entry-index/
File: sprites-entry-index.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 59/83



Author: Loïc *WydD* Petit
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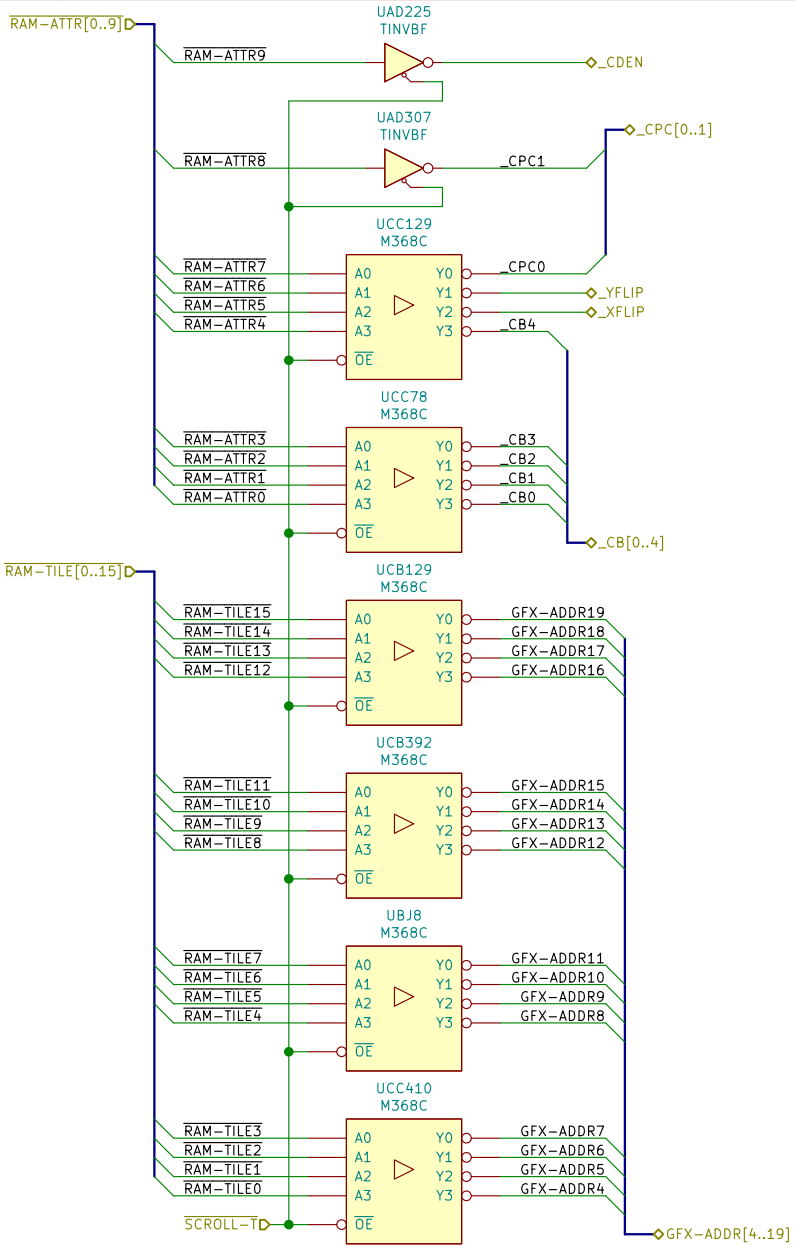
Sheet: /scroll-sram/
File: scroll-sram.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
KiCad E.D.A.	eeschema 5.1.7-a382d34a887ubuntu18.04.1	Id: 60/83



Author: Loïc *WydD* Petit
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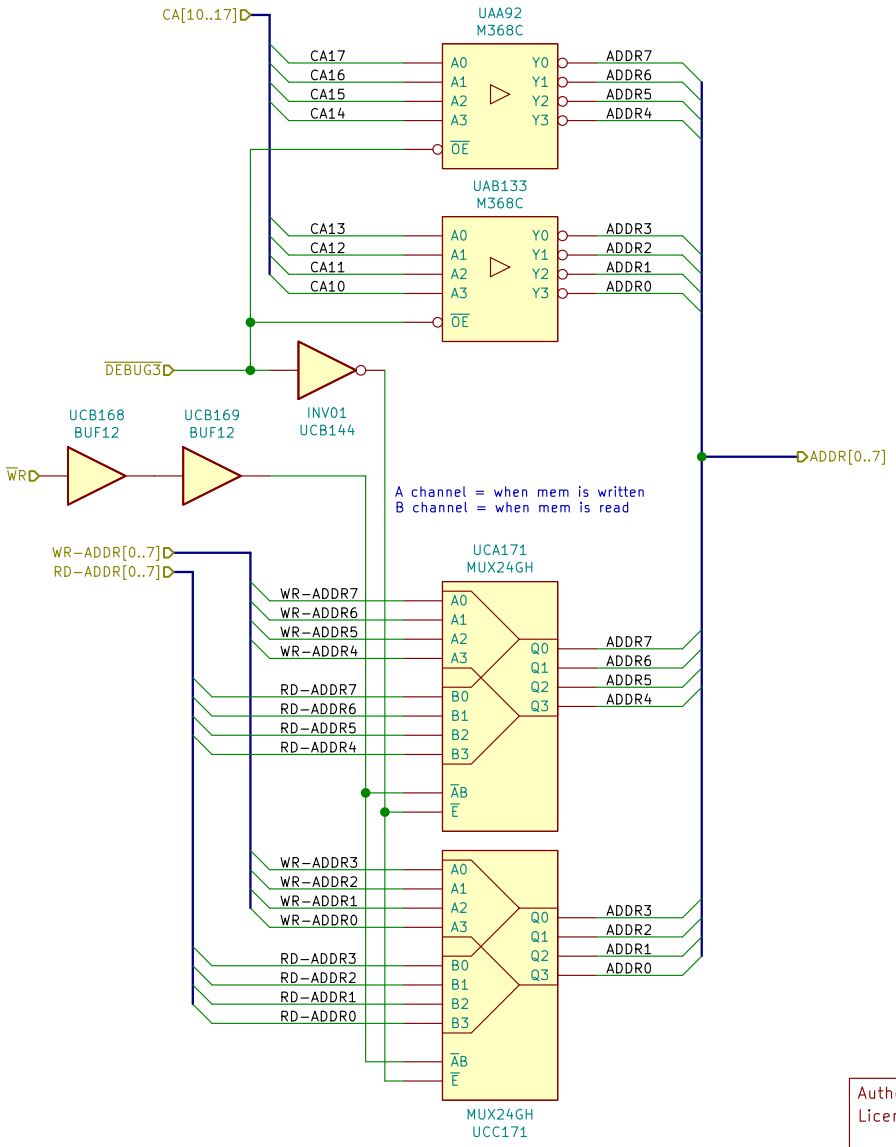
Sheet: /scroll-sram/scroll-roma/
File: scroll-roma.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 61/83



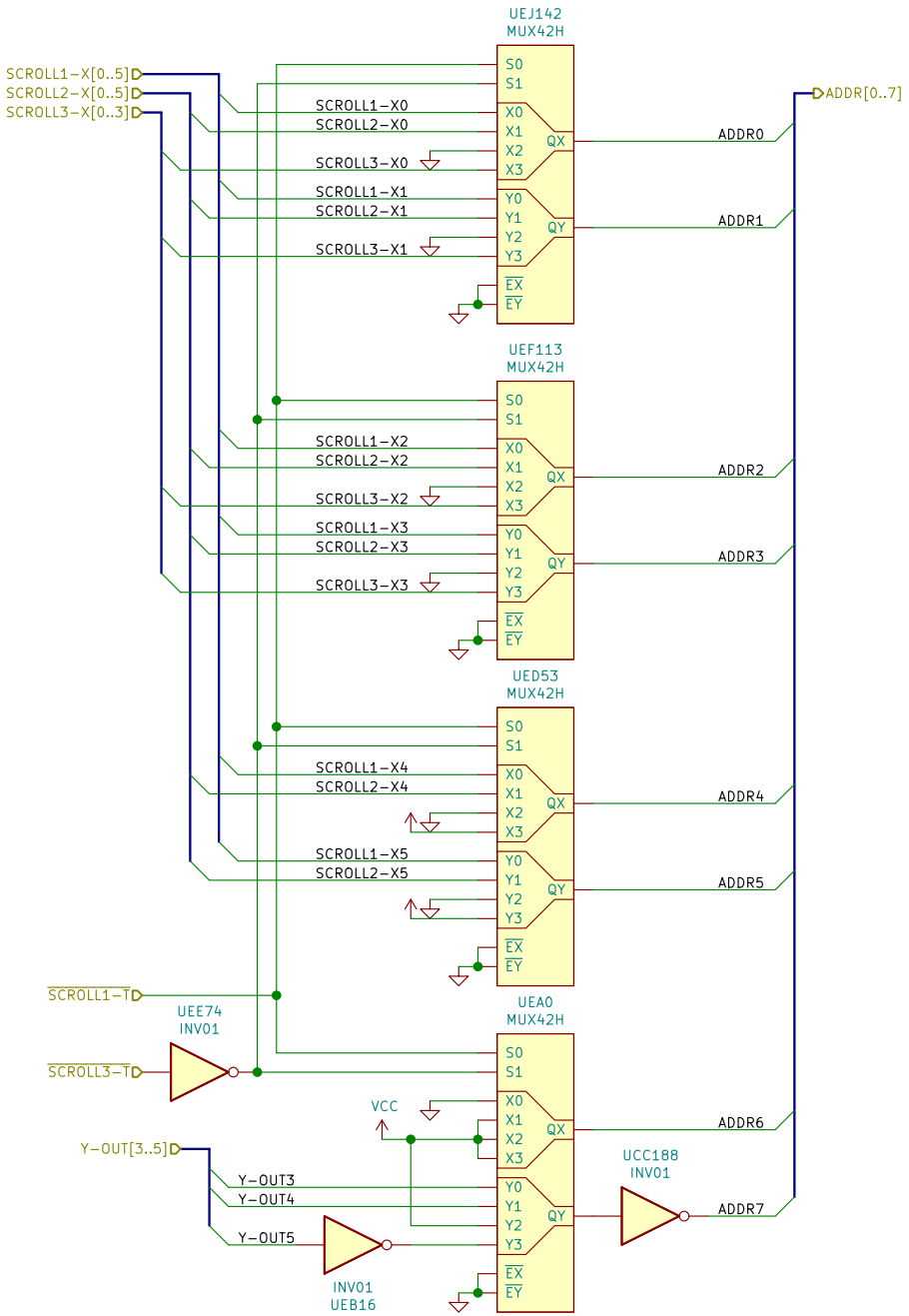
MEM-ADDR[7..0]

Author: Loïc *WydD* Petit
Licence: CC-BY

Sheet: /scroll-sram/sram-addr-mux/
File: sram-addr-mux.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 62/83



SCROLL1	SCROLL2	SCROLL3
Y3	Y4	Y5
0	1	1
X5	X5	1
X4	X4	1
X3	X3	X3
X2	X2	X2
X1	X1	X1
X0	X0	X0

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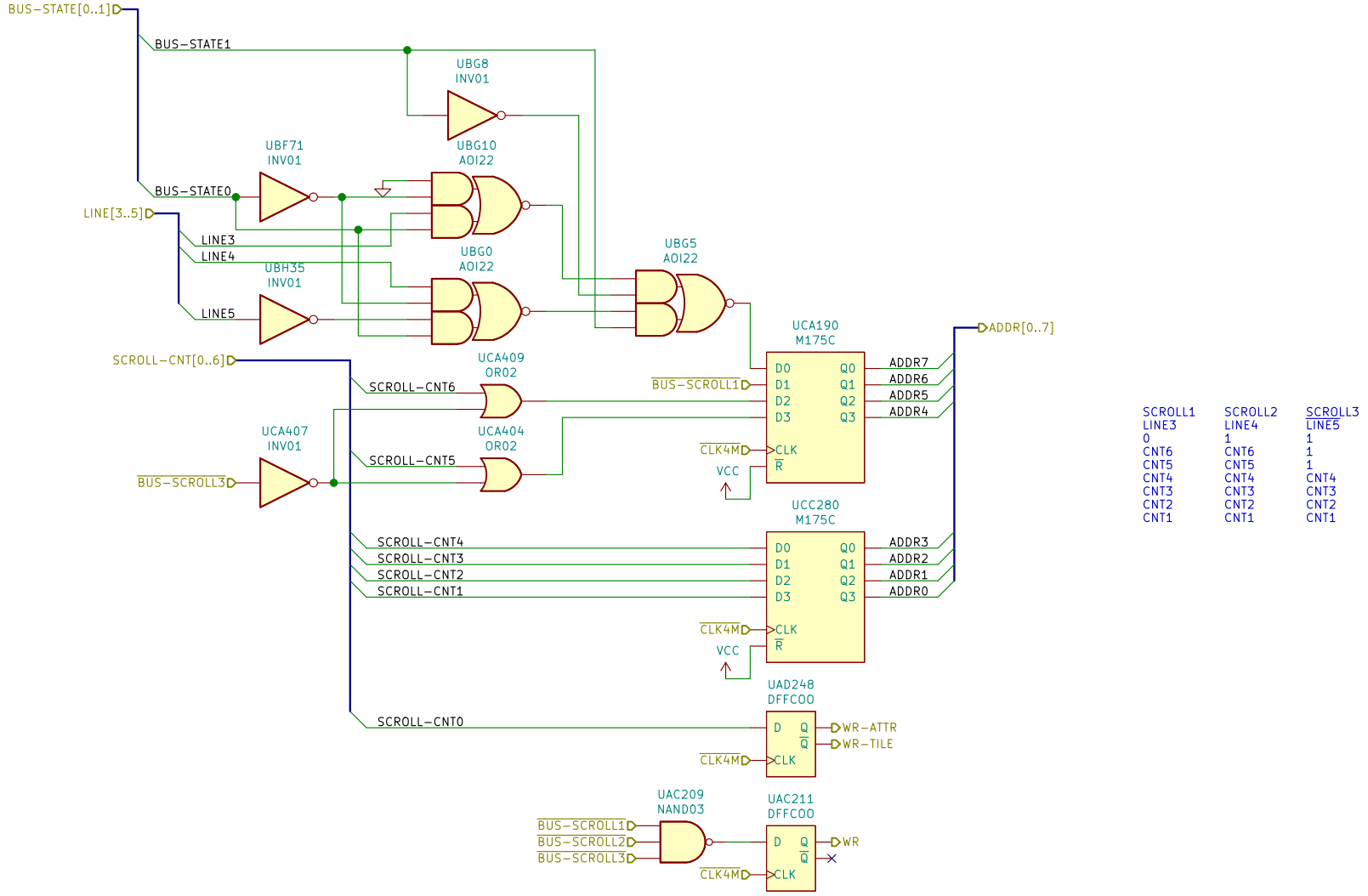
Sheet: /scroll-sram/sram-addr-read/
File: sram-addr-read.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
KiCad E.D.A. eeschema 5.1.7-a382d34a887ubuntu18.04.1		Id: 63/83



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File: sram-addr-write.sch

Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	**Rev:**
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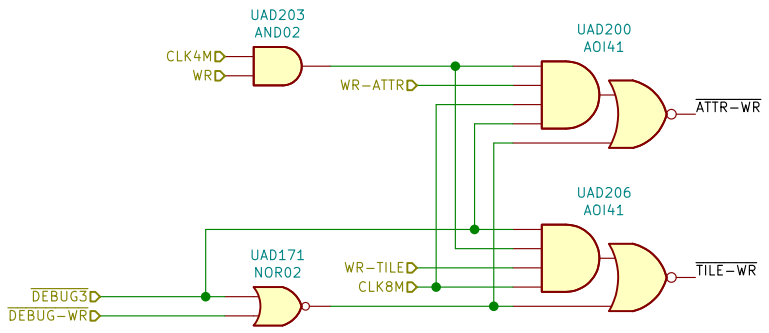
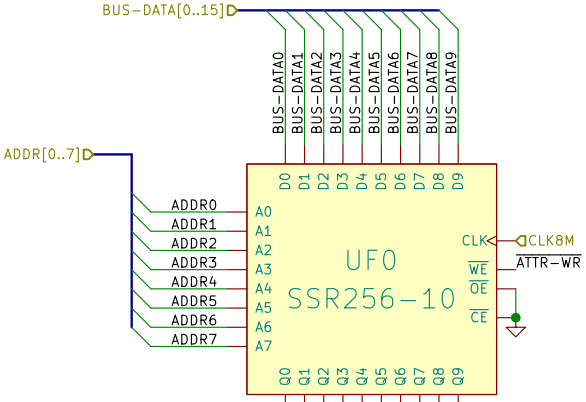
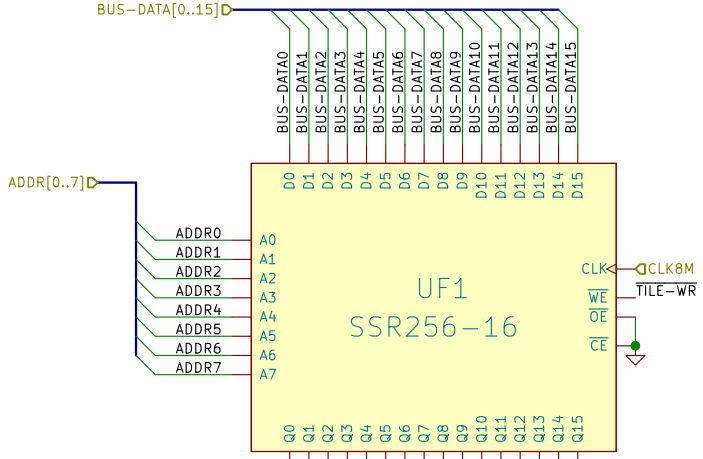
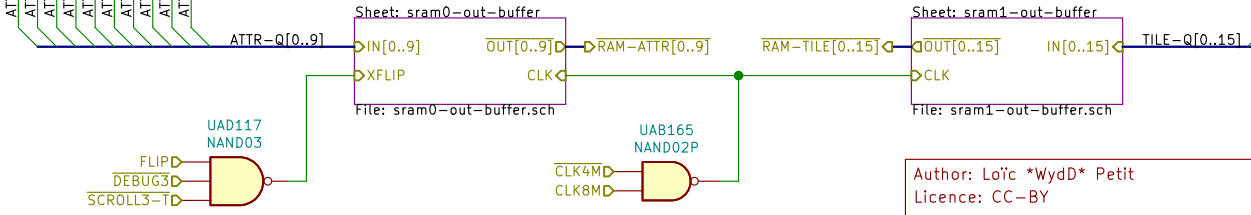
NOT [CLK4M & BUS-SCROLL@$\overline{CLK4M}$ & CNT0@$\overline{CLK4M}$ & CLK8M & $\overline{DEBUG3}$]









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File: sram1.sch

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Size: A4	Date: 2021-09-12	Rev:
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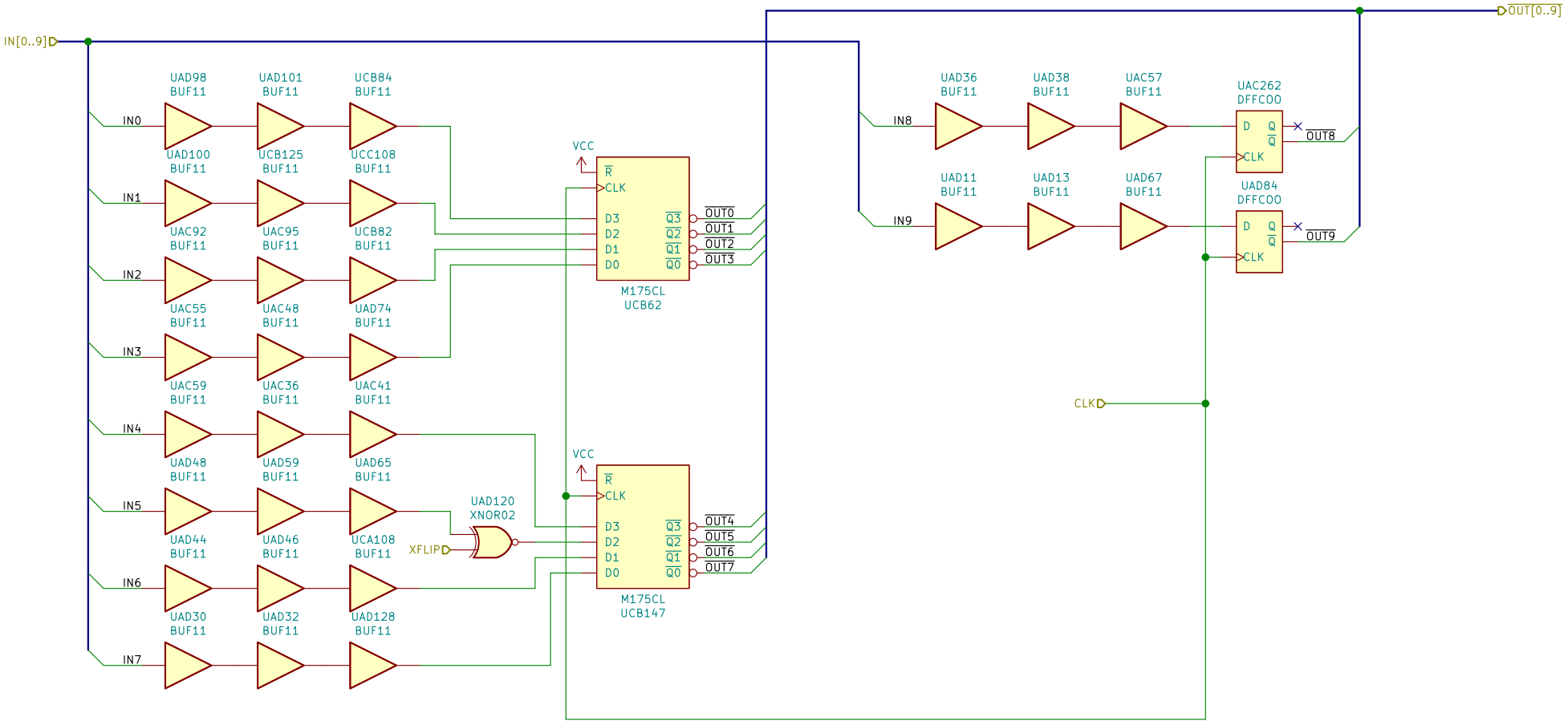

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Sheet: /scroll-sram/sram1/sram0-out-buffer/
File: sram0-out-buffer.sch

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Size: A4	Date: 2021-09-12	**Rev:**
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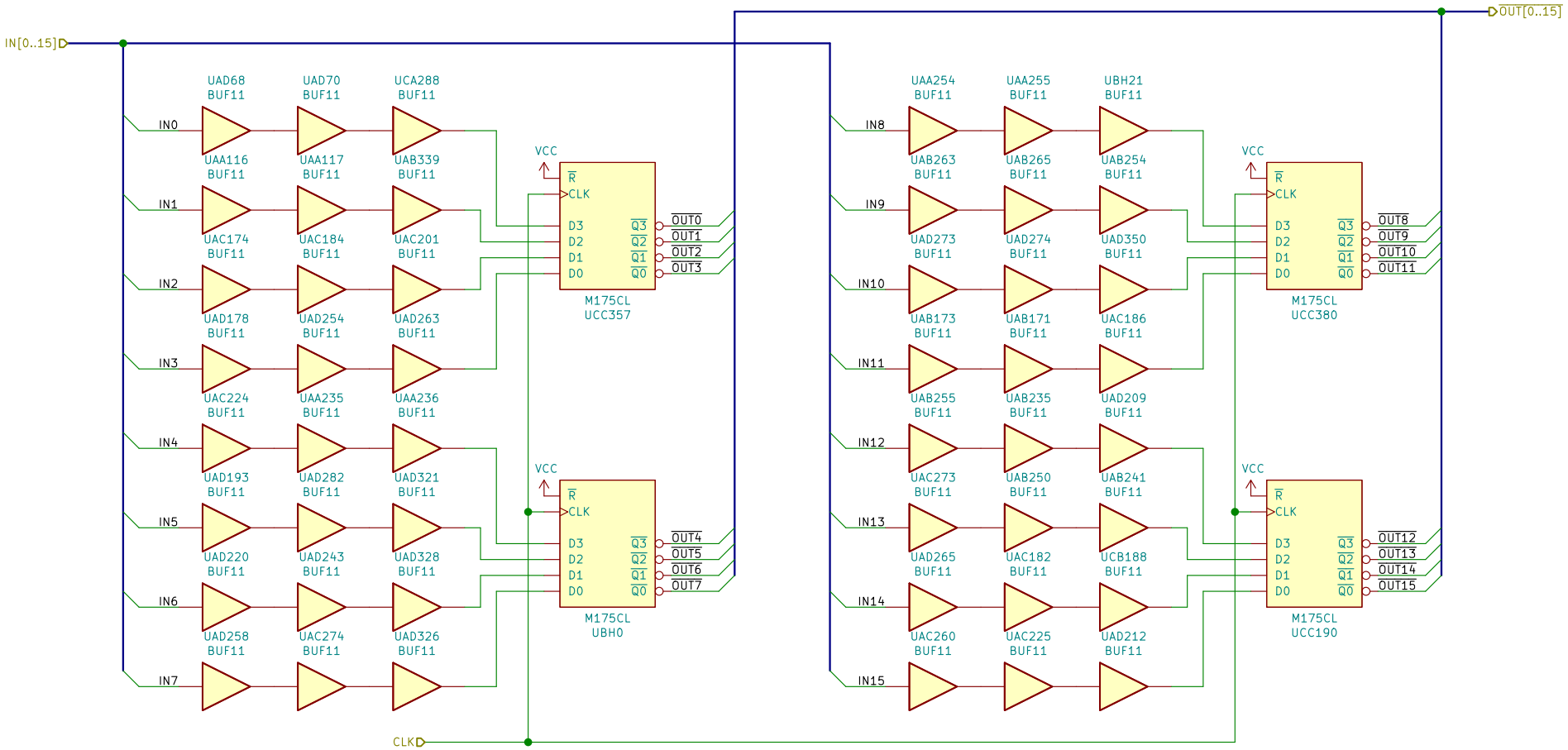

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Sheet: /scroll-sram/sram1/sram1-out-buffer/
File: sram1-out-buffer.sch

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Size: A4	Date: 2021-09-12	**Rev:**
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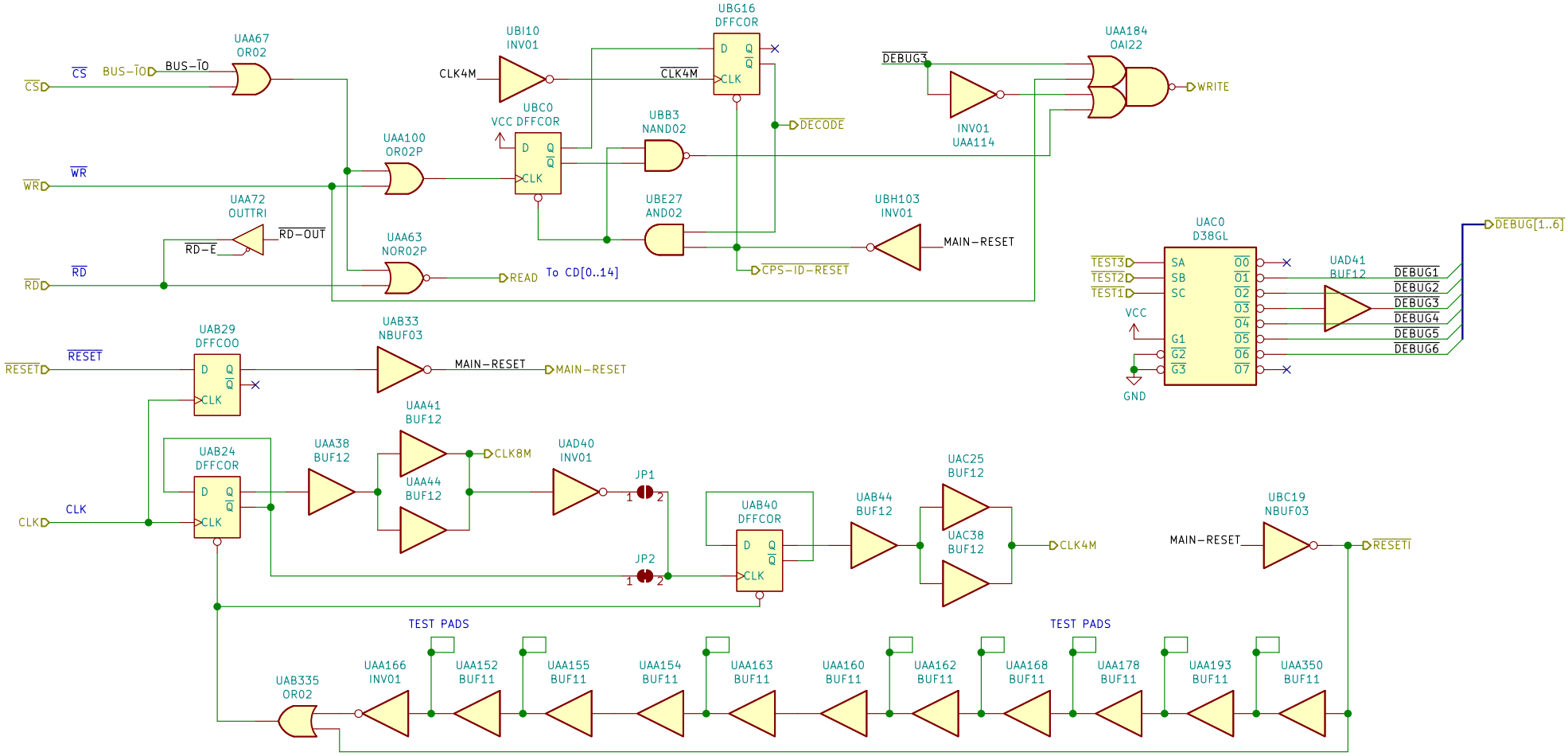

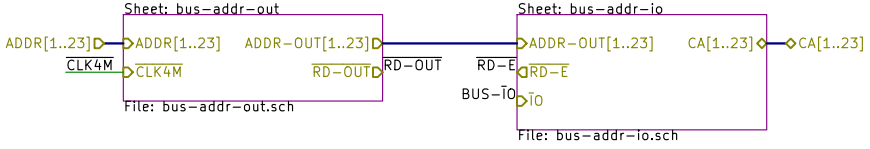

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Sheet: /main-signals/
File: main-signals.sch

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Size: A4	Date: 2021-09-12	**Rev:**
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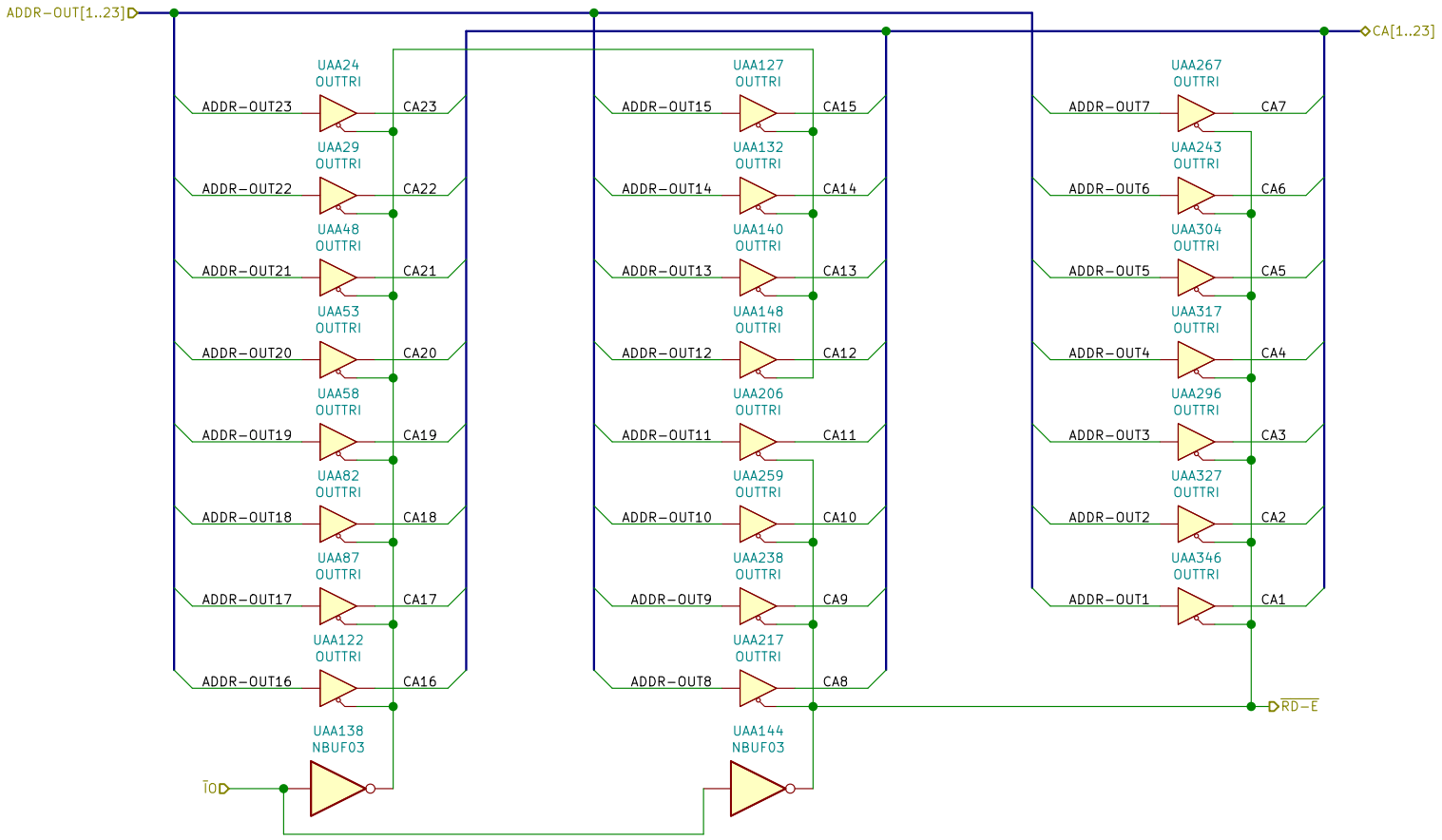

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File: bus-addr-io.sch

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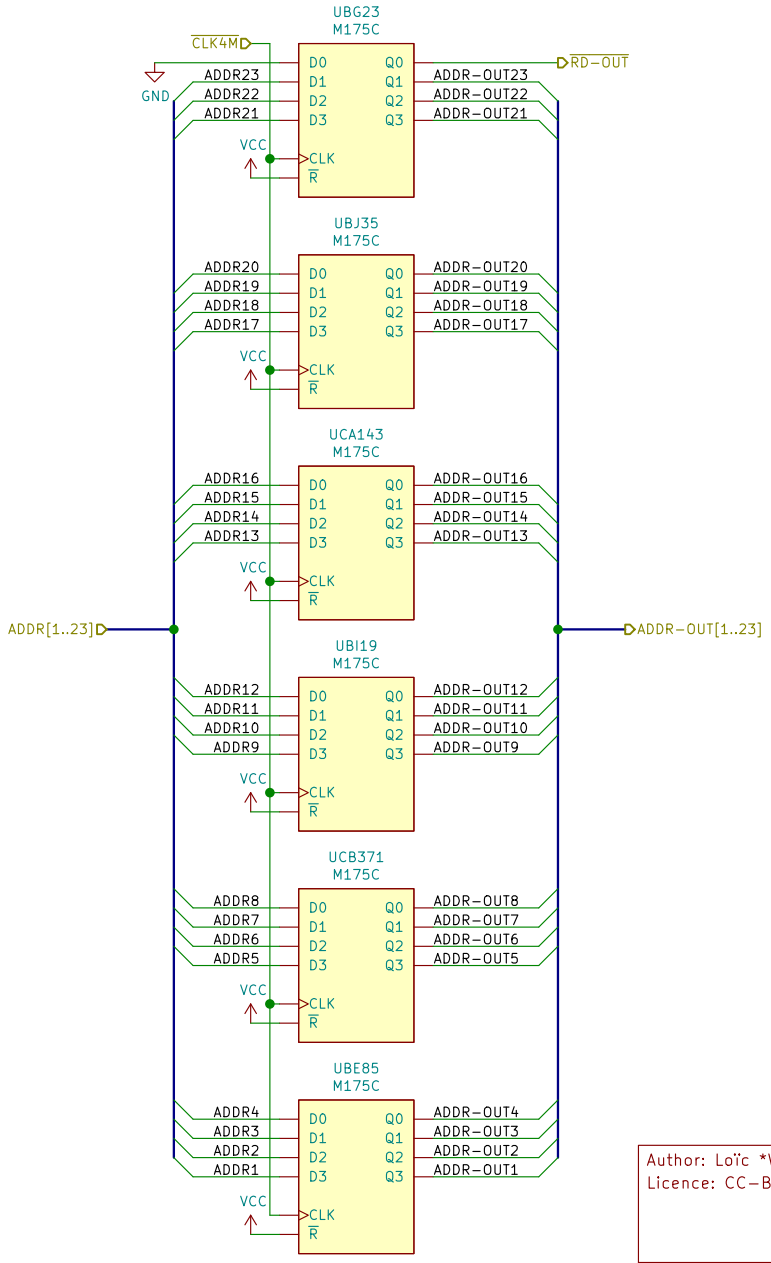

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Sheet: /main-signals/bus-addr-out/
File: bus-addr-out.sch

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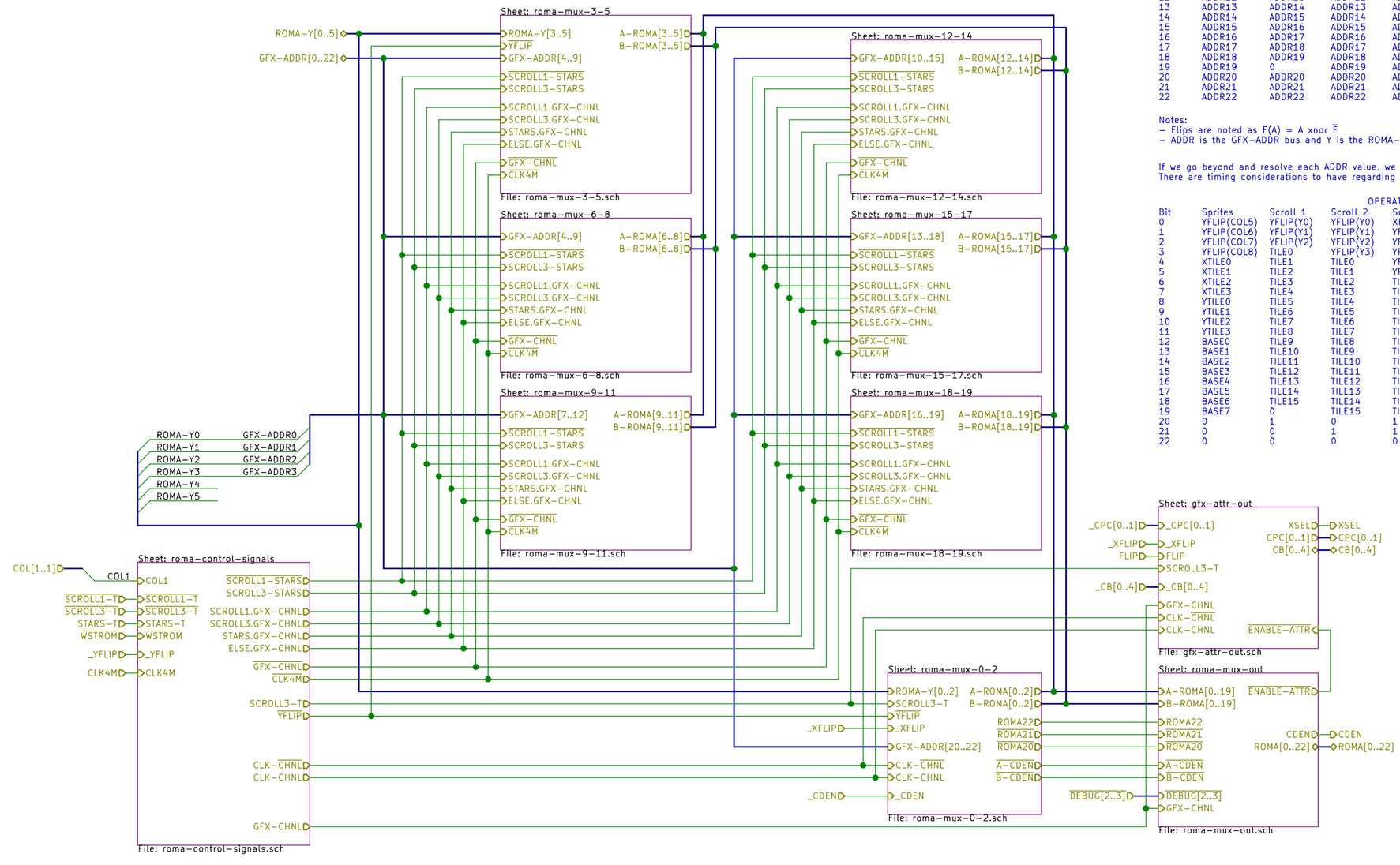

This part is a big and complex bus multiplexer.
Sometimes it has clear distinct lines, sometimes processing are mutualized between layers.
For the sake of clarity, I've layed down what is the result of the ROMA bus
after everything is applied (assuming no DEBUG flag)

OPERATIONS

ROMA	Sprites	Scroll 1	Scroll 2	Scroll 3	Star 1	Star 2	WSTROM
0	YFLIP(Y0)	YFLIP(Y0)	YFLIP(Y0)	XFLIP(Y0)	Y0	Y0	ADDR0
1	YFLIP(Y1)	YFLIP(Y1)	YFLIP(Y1)	YFLIP(Y1)	Y1	Y1	ADDR1
2	YFLIP(Y2)	YFLIP(Y2)	YFLIP(Y2)	YFLIP(Y2)	Y2	Y2	ADDR2
3	YFLIP(Y3)	ADDR4	YFLIP(Y3)	YFLIP(Y3)	Y3	Y3	ADDR3
4	ADDR4	ADDR5	ADDR4	YFLIP(Y4)	Y4	Y4	ADDR4
5	ADDR5	ADDR6	ADDR5	YFLIP(Y5)	ADDR4	ADDR4	ADDR5
6	ADDR6	ADDR7	ADDR6	ADDR4	ADDR5	ADDR5	ADDR6
7	ADDR7	ADDR8	ADDR7	ADDR5	ADDR6	ADDR6	ADDR7
8	ADDR8	ADDR9	ADDR8	ADDR6	ADDR7	ADDR7	ADDR8
9	ADDR9	ADDR10	ADDR9	ADDR7	ADDR8	ADDR8	ADDR9
10	ADDR10	ADDR11	ADDR10	ADDR8	ADDR9	ADDR9	ADDR10
11	ADDR11	ADDR12	ADDR11	ADDR9	ADDR10	ADDR10	ADDR11
12	ADDR12	ADDR13	ADDR12	ADDR10	ADDR11	ADDR11	ADDR12
13	ADDR13	ADDR14	ADDR13	ADDR11	ADDR12	ADDR12	ADDR13
14	ADDR14	ADDR15	ADDR14	ADDR12	ADDR13	ADDR13	ADDR14
15	ADDR15	ADDR16	ADDR15	ADDR13	ADDR14	ADDR14	ADDR15
16	ADDR16	ADDR17	ADDR16	ADDR14	ADDR15	ADDR15	ADDR16
17	ADDR17	ADDR18	ADDR17	ADDR15	ADDR16	ADDR16	ADDR17
18	ADDR18	ADDR19	ADDR18	ADDR16	ADDR17	ADDR17	ADDR18
19	ADDR19	0	ADDR19	ADDR17	ADDR18	ADDR18	ADDR19
20	ADDR20	ADDR20	ADDR20	ADDR20	ADDR20	ADDR20	ADDR20
21	ADDR21	ADDR21	ADDR21	ADDR21	ADDR21	ADDR21	ADDR21
22	ADDR22	ADDR22	ADDR22	ADDR22	ADDR22	ADDR22	ADDR22

Notes:
- Flips are noted as F(A) = A xnor $\overline{F}$
- ADDR is the GFX-ADDR bus and Y is the ROMA-Y bus

If we go beyond and resolve each ADDR value, we get the following lookup table
There are timing considerations to have regarding the channel but the overall idea is there.

OPERATIONS

Bit	Sprites	Scroll 1	Scroll 2	Scroll 3	Star 1	Star 2	WSTROM
0	YFLIP(COL5)	YFLIP(Y0)	YFLIP(Y0)	XFLIP(X1)	Y0	Y0	CNT0
1	YFLIP(COL6)	YFLIP(Y1)	YFLIP(Y1)	YFLIP(Y0)	Y1	Y1	CNT1
2	YFLIP(COL7)	YFLIP(Y2)	YFLIP(Y2)	YFLIP(Y1)	Y2	Y2	CNT2
3	YFLIP(COL8)	TILE0	YFLIP(Y3)	YFLIP(Y2)	Y3	Y3	CNT3
4	XTILE0	TILE1	TILE0	YFLIP(Y3)	Y4	Y4	CNT4
5	XTILE1	TILE2	TILE1	YFLIP(Y4)	Y5	Y5	CNT5
6	XTILE2	TILE3	TILE2	TILE0	Y6	Y6	CNT6
7	XTILE3	TILE4	TILE3	TILE1	Y7	Y7	CNT7
8	YTILE0	TILE5	TILE4	TILE2	STARX0	STARX0	CNT8
9	YTILE1	TILE6	TILE5	TILE3	STARX1	STARX1	CNT9
10	YTILE2	TILE7	TILE6	TILE4	STARX2	STARX2	CNT10
11	YTILE3	TILE8	TILE7	TILE5	STARX3	STARX3	CNT11
12	BASE0	TILE9	TILE8	TILE6	Y8	Y8	CNT12
13	BASE1	TILE10	TILE9	TILE7	0	0	CNT13
14	BASE2	TILE11	TILE10	TILE8	0	0	CNT14
15	BASE3	TILE12	TILE11	TILE9	0	0	CNT15
16	BASE4	TILE13	TILE12	TILE10	0	0	CNT16
17	BASE5	TILE14	TILE13	TILE11	0	0	CNT17
18	BASE6	TILE15	TILE14	TILE12	0	0	CNT18
19	BASE7	0	TILE15	TILE13	0	0	CNT19
20	0	1	0	1	0	0	CNT20
21	0	0	1	1	0	0	CNT21
22	0	0	0	0	1	1	CNT22

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Sheet: /raster-out/
File: raster-out.sch

Title: CPS Reverse Engineering: DL-0311

Size: A3	Date: 2021-09-12	**Rev:**
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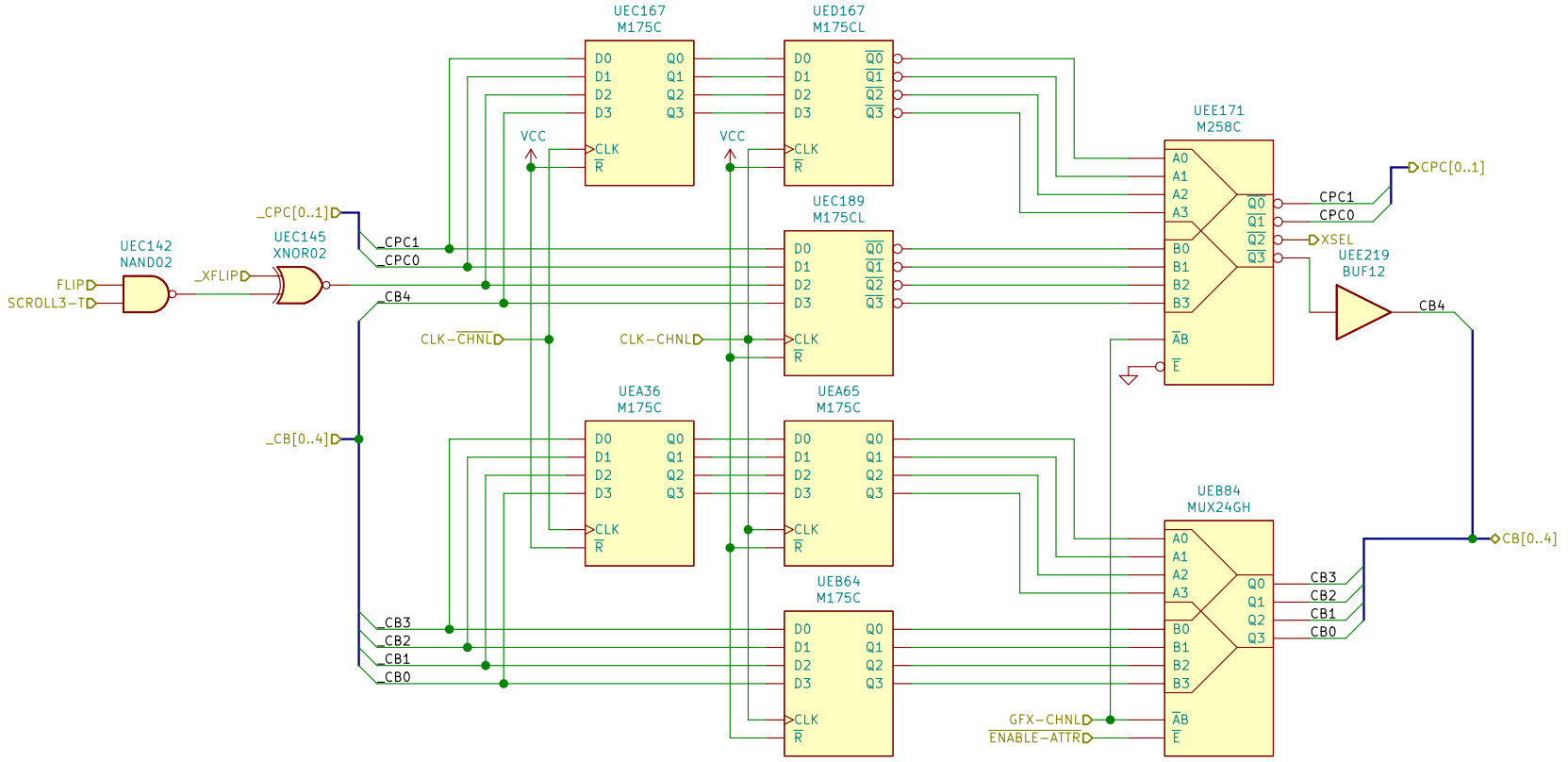

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Title: CPS Reverse Engineering: DL-0311

Size: A4	Date: 2021-09-12	Rev:
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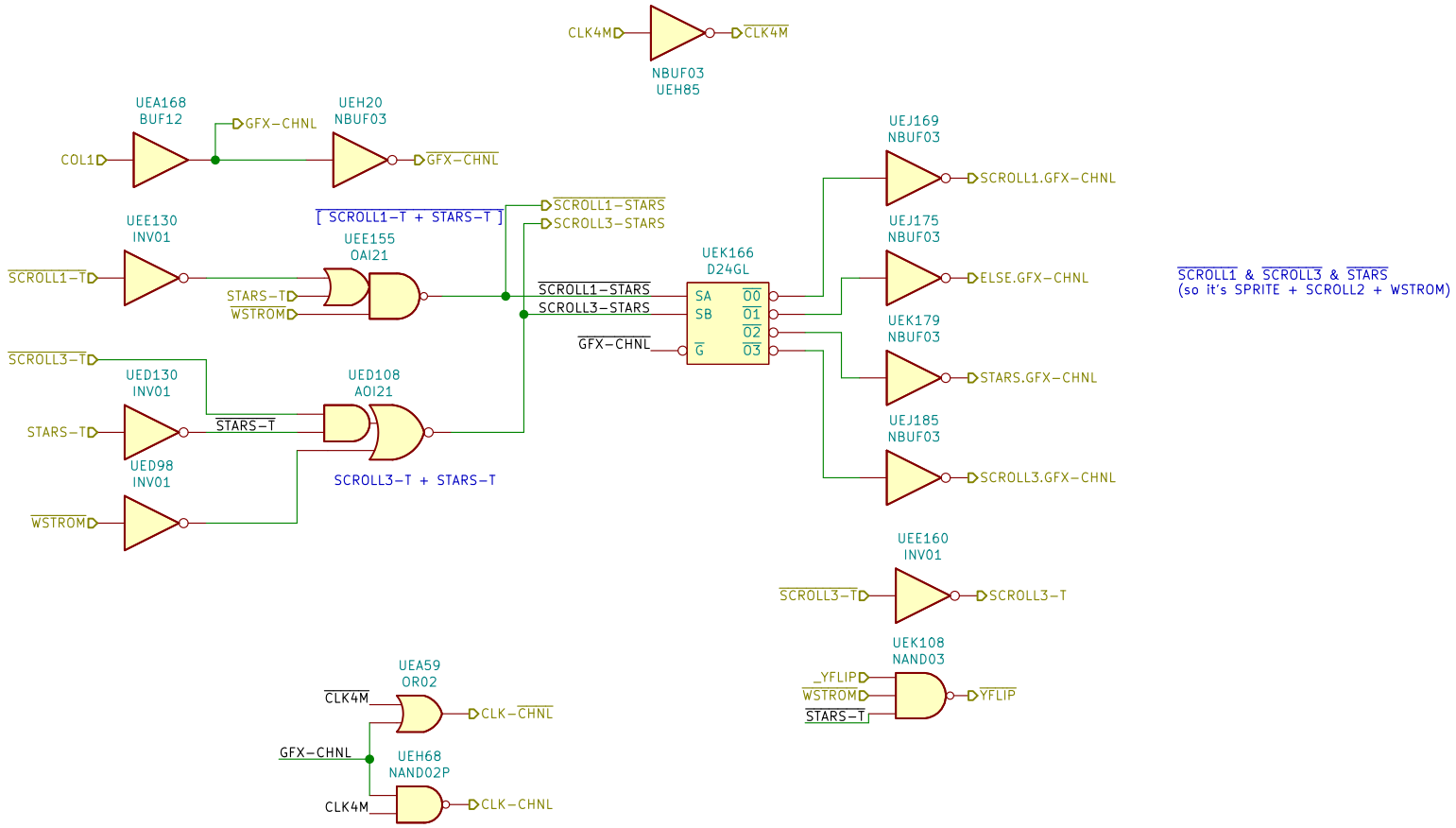

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Size: A4	Date: 2021-09-12	Rev:
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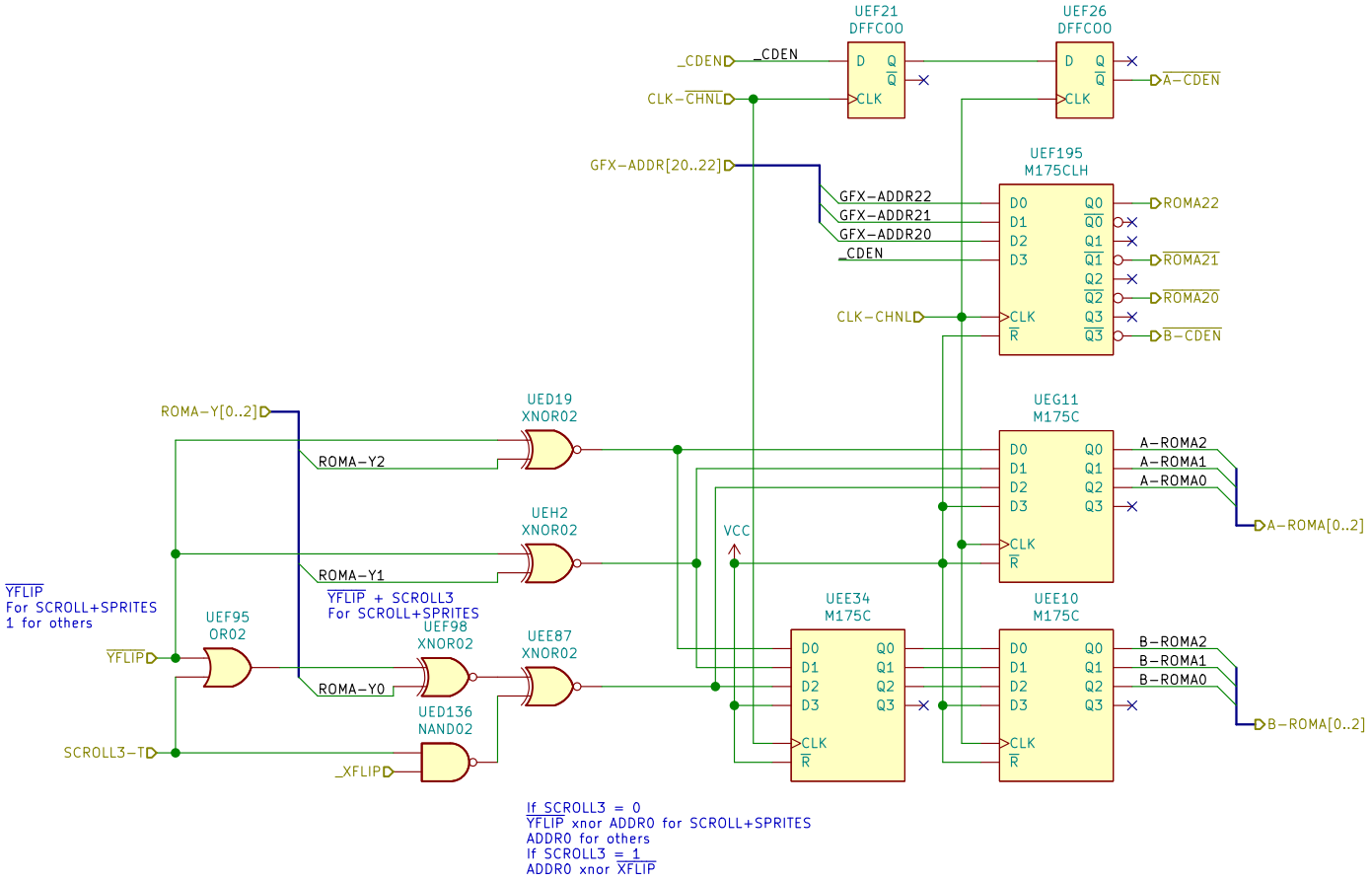

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File: roma-mux-0-2.sch

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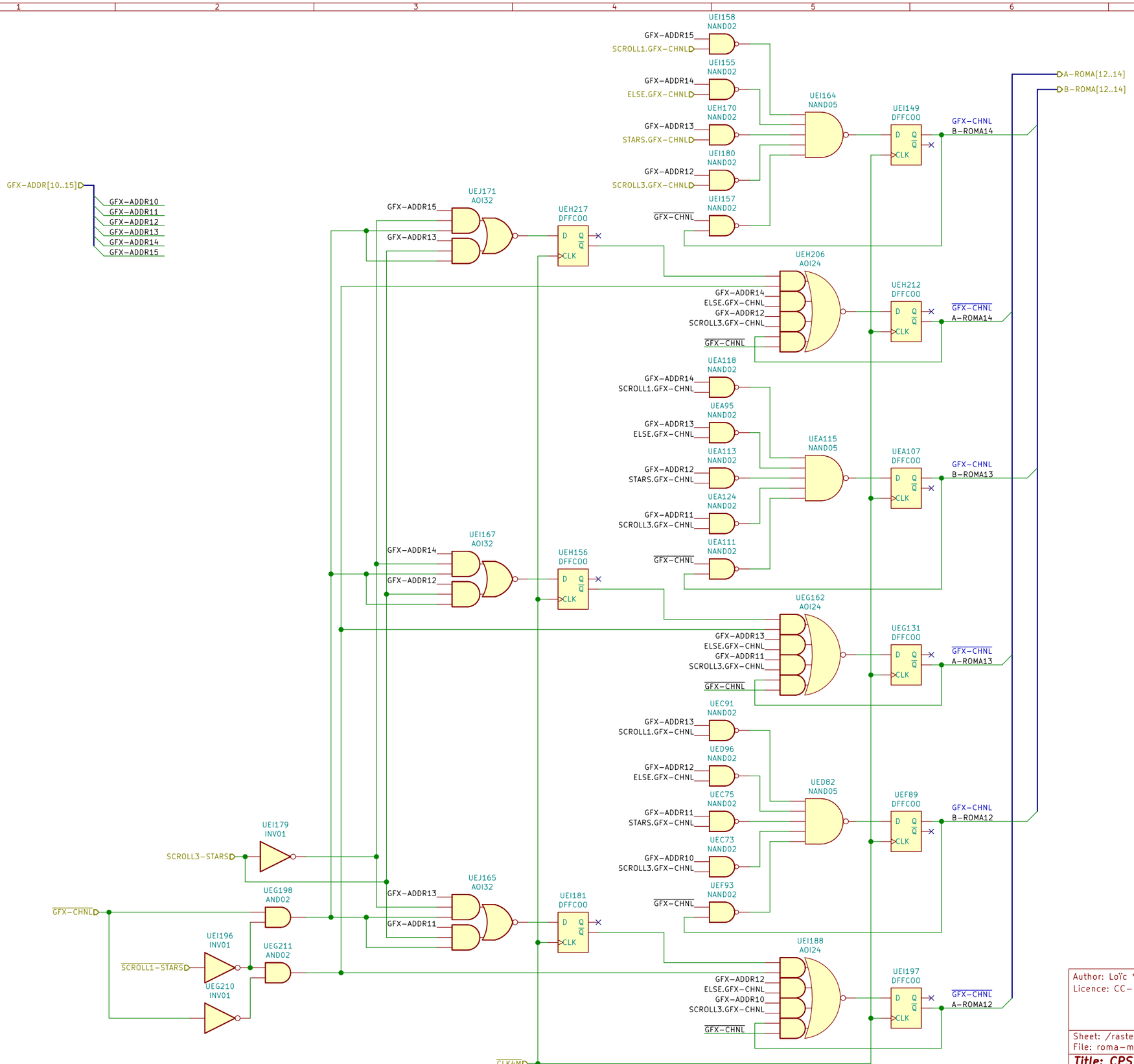

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File: roma-mux-12-14.sch

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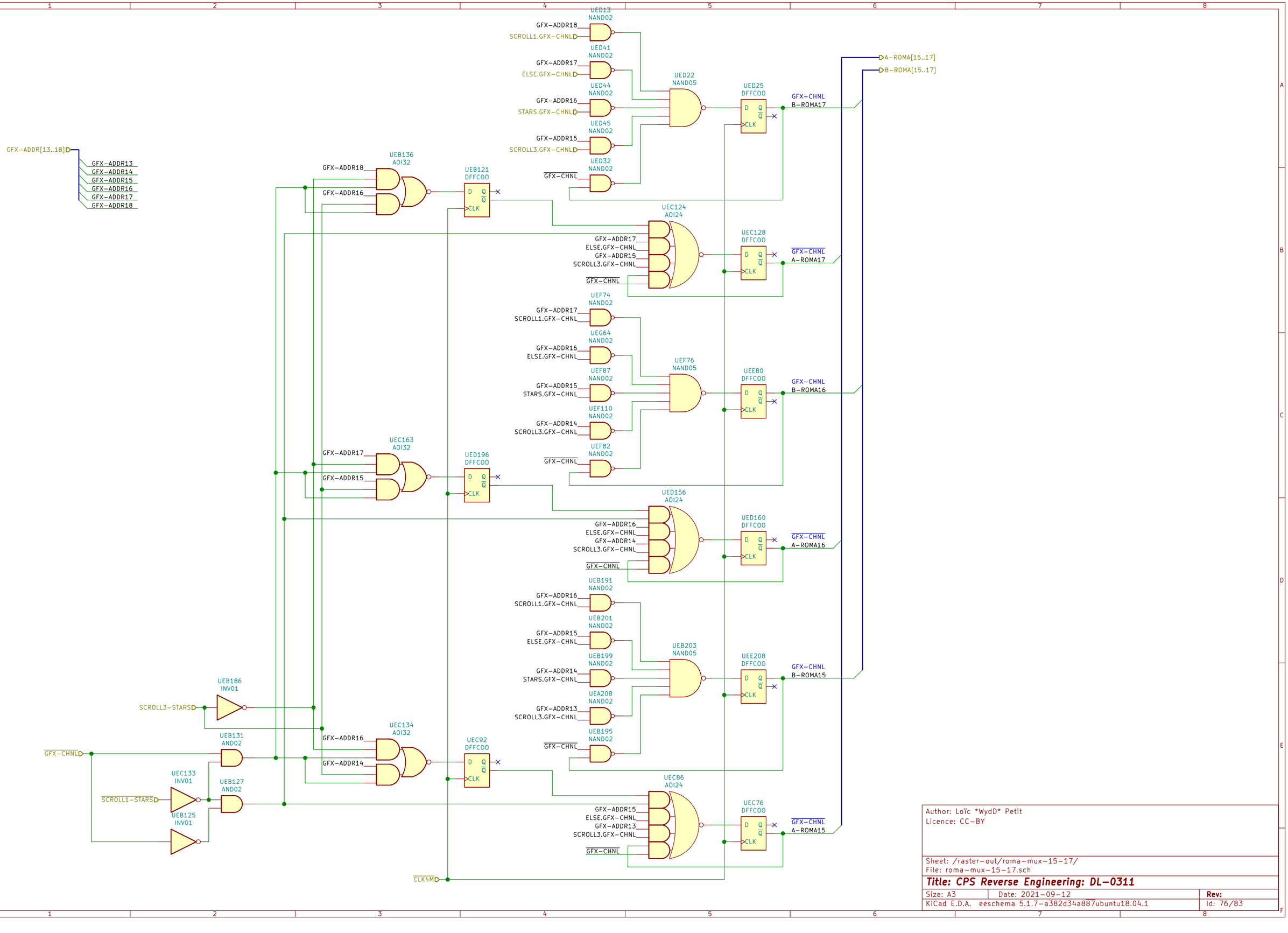

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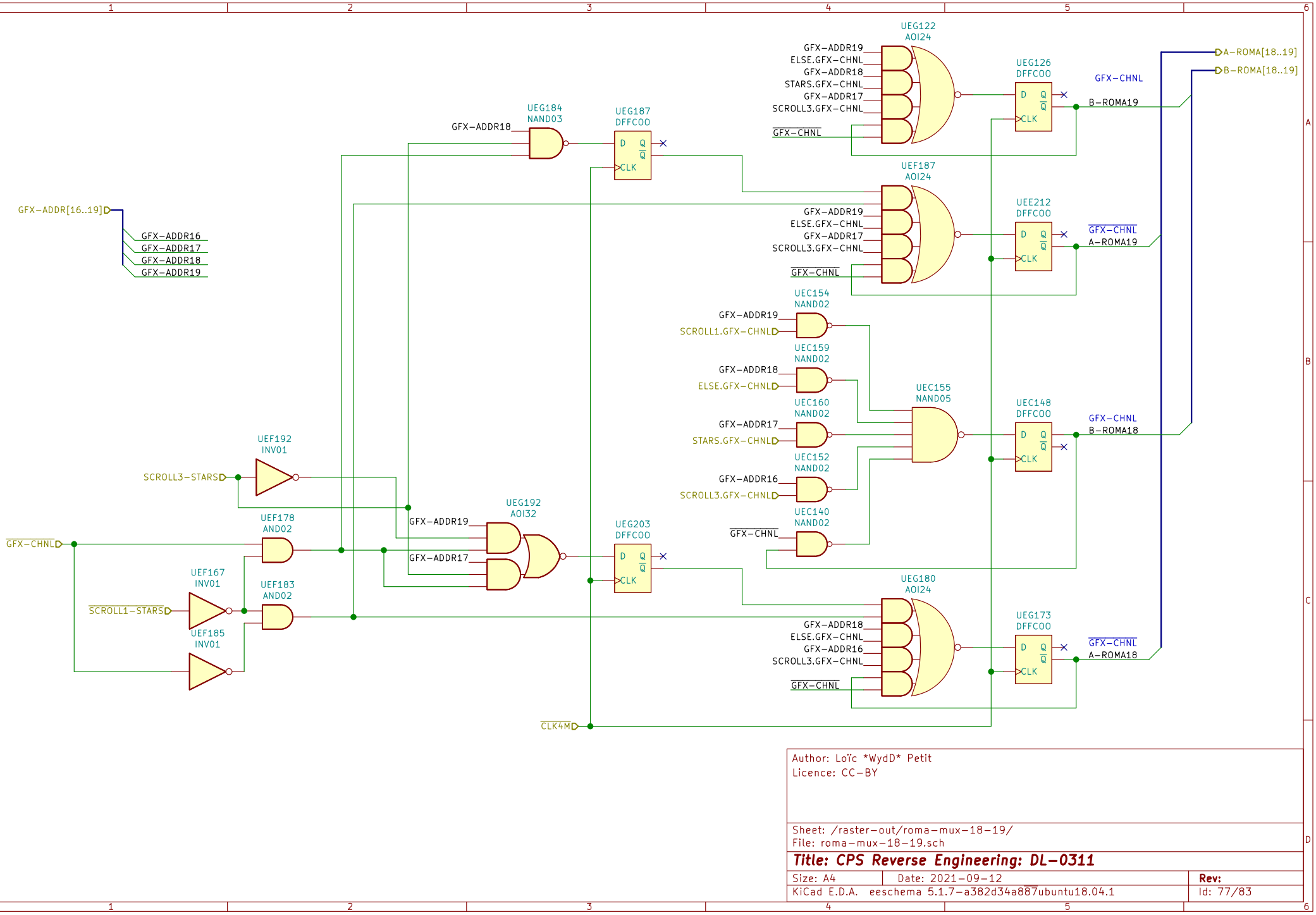

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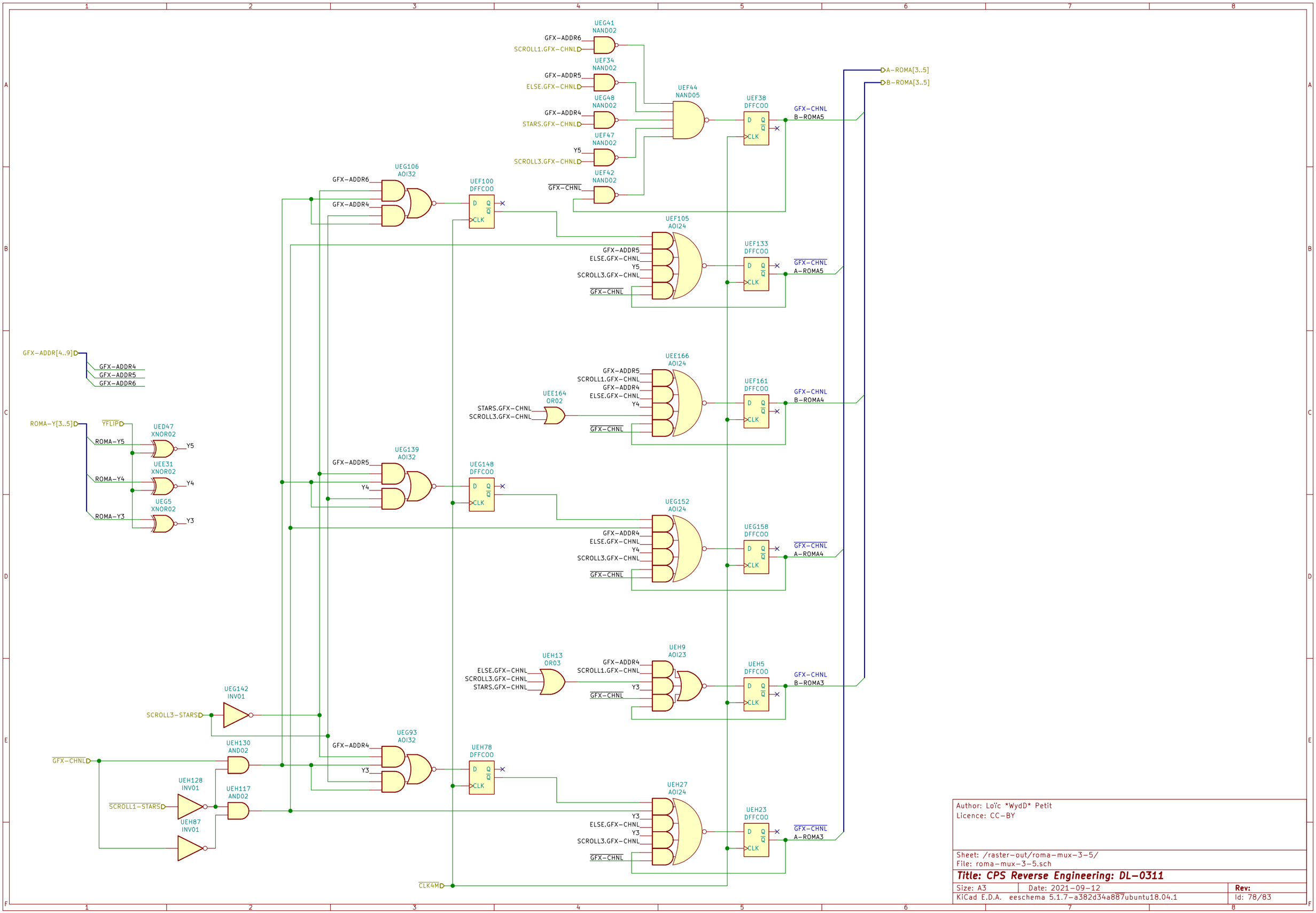

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Size: A3	Date: 2021-09-12	Rev:
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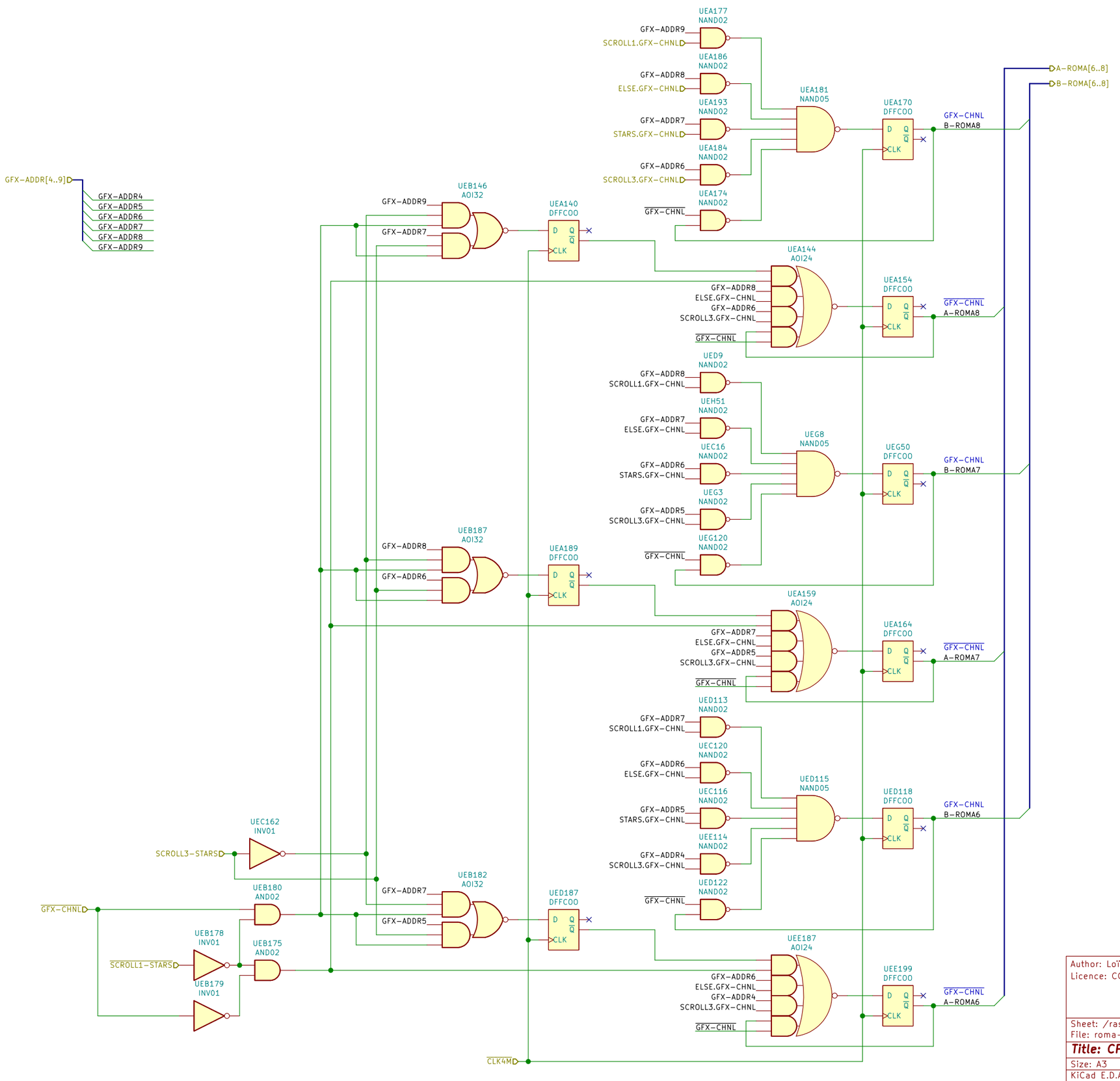
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GFX-ADDR5
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GFX-ADDR9
UEA177 NAND02
GFX-ADDR9
SCROLL1.GFX-CHNL
UEA186 NAND02
GFX-ADDR8
ELSE.GFX-CHNL
UEA193 NAND02
GFX-ADDR7
STARS.GFX-CHNL
UEA184 NAND02
GFX-ADDR6
SCROLL3.GFX-CHNL
UEA174 NAND02
GFX-CHNL
UEA181 NAND05
UEA170 DFFCOO
D Q
CLK
GFX-CHNL
B-ROMA8
A-ROMA[6..8]
B-ROMA[6..8]
UEB146 AOI32
GFX-ADDR9
GFX-ADDR7
UEA140 DFFCOO
UEA144 AOI24
GFX-ADDR8
ELSE.GFX-CHNL
GFX-ADDR6
SCROLL3.GFX-CHNL
GFX-CHNL
UEA154 DFFCOO
GFX-CHNL
A-ROMA8
UED9 NAND02
GFX-ADDR8
SCROLL1.GFX-CHNL
UEH51 NAND02
GFX-ADDR7
ELSE.GFX-CHNL
UEC16 NAND02
GFX-ADDR6
STARS.GFX-CHNL
UEG3 NAND02
GFX-ADDR5
SCROLL3.GFX-CHNL
UEG120 NAND02
GFX-CHNL
UEG8 NAND05
UEG50 DFFCOO
GFX-CHNL
B-ROMA7
UEB187 AOI32
GFX-ADDR8
GFX-ADDR6
UEA189 DFFCOO
UEA159 AOI24
GFX-ADDR7
ELSE.GFX-CHNL
GFX-ADDR5
SCROLL3.GFX-CHNL
GFX-CHNL
UEA164 DFFCOO
GFX-CHNL
A-ROMA7
UED113 NAND02
GFX-ADDR7
SCROLL1.GFX-CHNL
UEC120 NAND02
GFX-ADDR6
ELSE.GFX-CHNL
UEC116 NAND02
GFX-ADDR5
STARS.GFX-CHNL
UEE114 NAND02
GFX-ADDR4
SCROLL3.GFX-CHNL
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GFX-CHNL
UED115 NAND05
UED118 DFFCOO
GFX-CHNL
B-ROMA6
UEC162 INV01
SCROLL3-STARS
UEB180 AND02
GFX-CHNL
UEB178 INV01
SCROLL1-STARS
UEB175 AND02
UEB179 INV01
UEB182 AOI32
GFX-ADDR7
GFX-ADDR5
UED187 DFFCOO
UEE187 AOI24
GFX-ADDR6
ELSE.GFX-CHNL
GFX-ADDR4
SCROLL3.GFX-CHNL
GFX-CHNL
UEE199 DFFCOO
GFX-CHNL
A-ROMA6
CLK4M
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File: roma-mux-6-8.sch
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Size: A3
Date: 2021-09-12
Rev:
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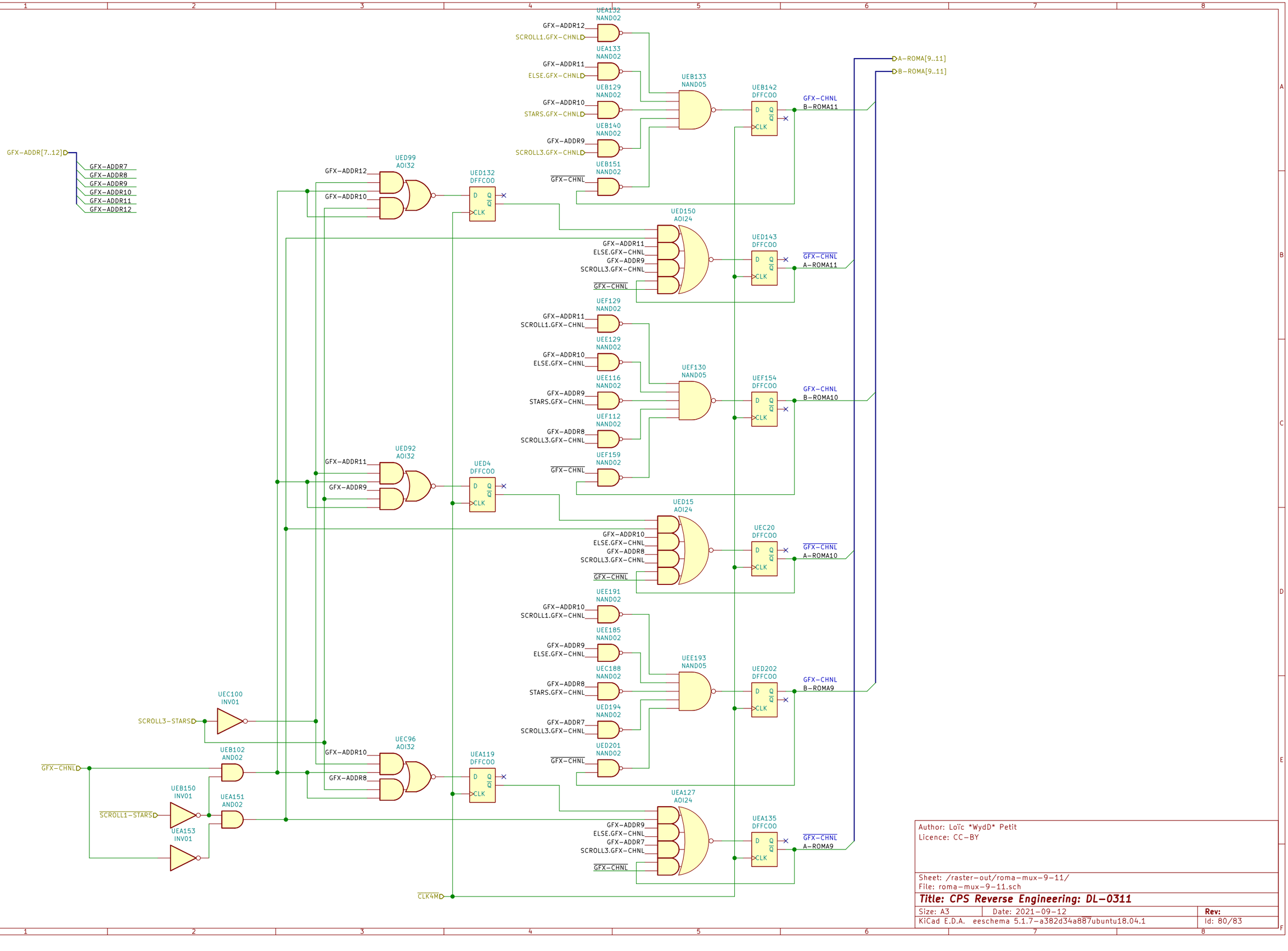

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File: roma-mux-9-11.sch

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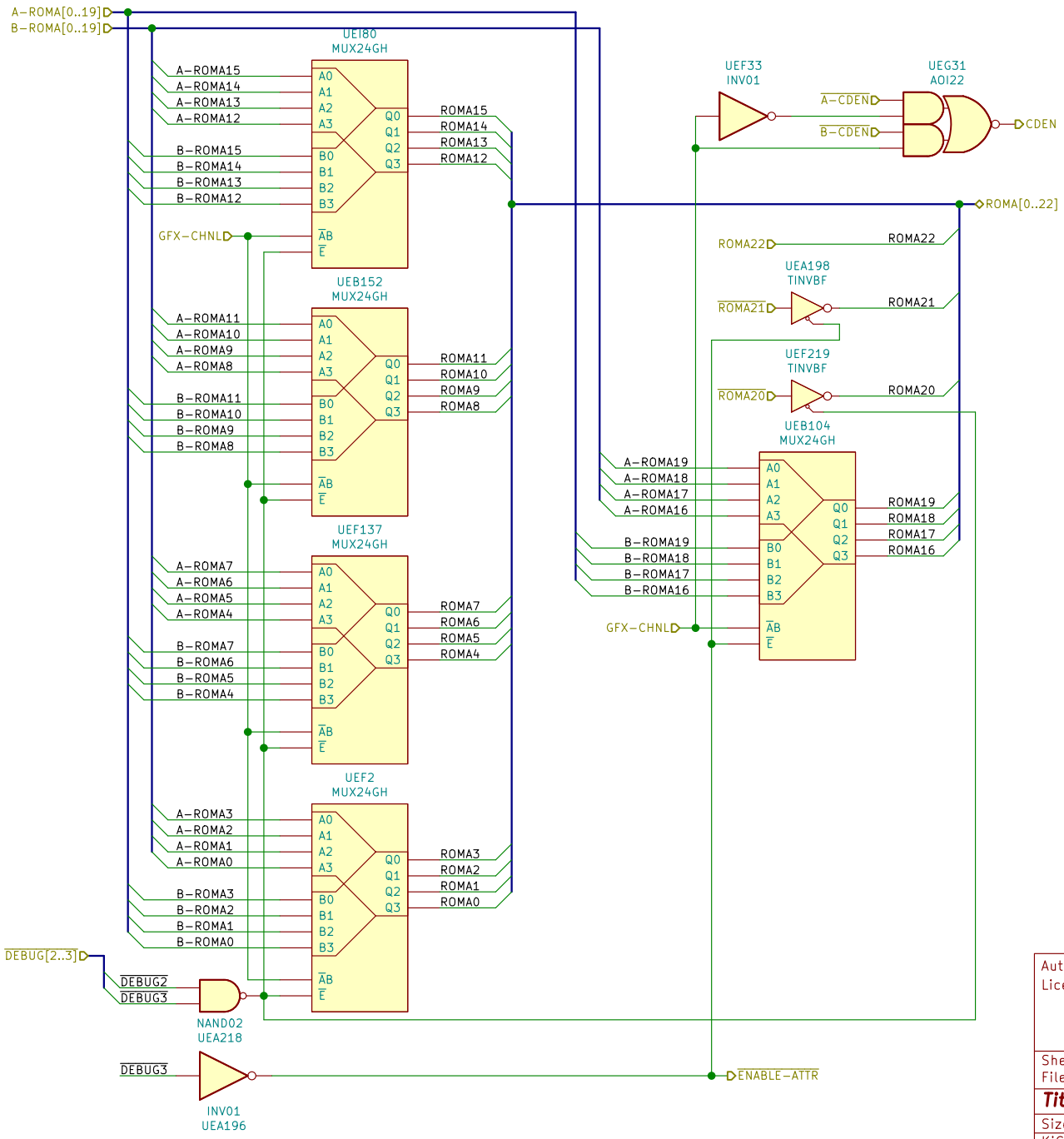

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File: roma-mux-out.sch

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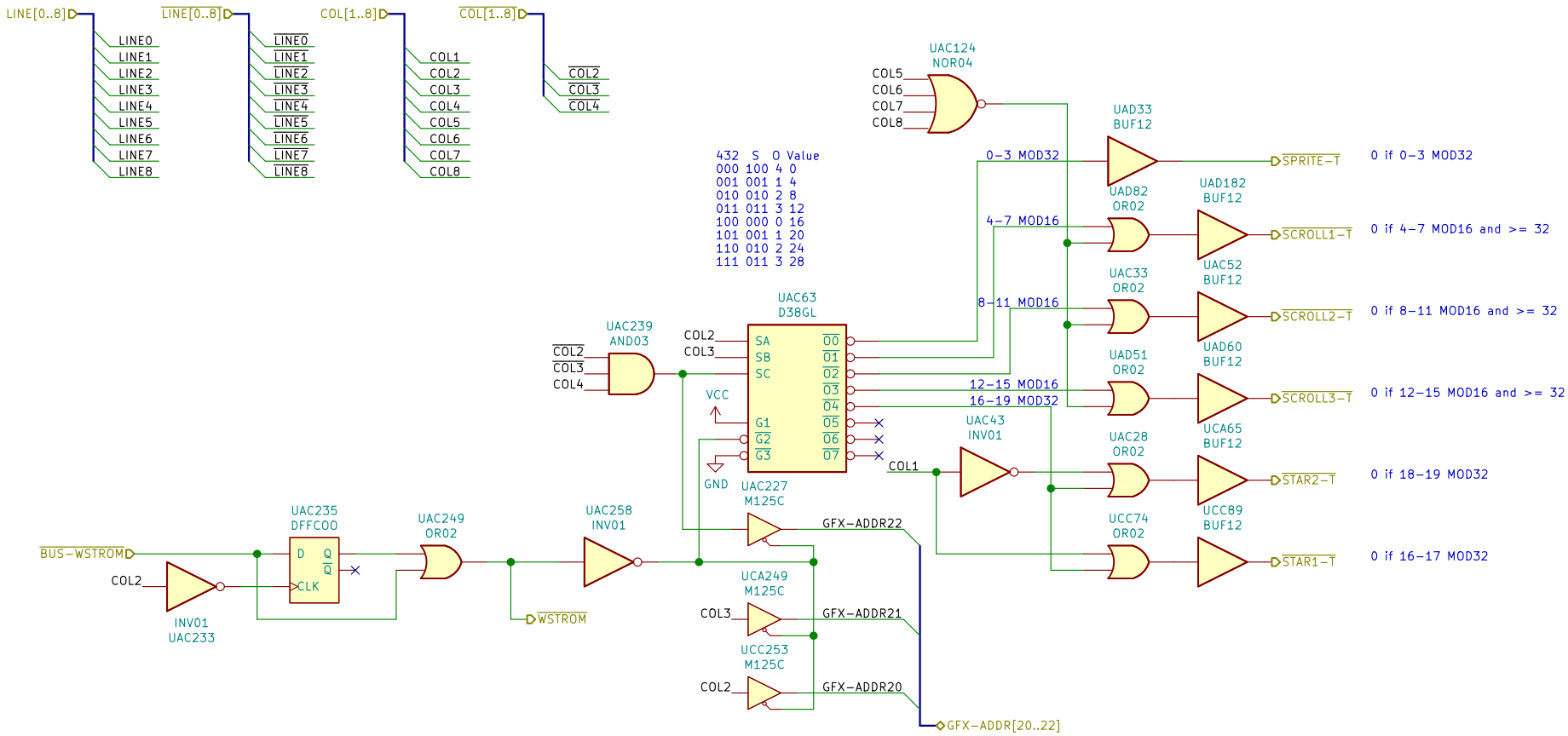

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File: video-timings.sch

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Size: A4	Date: 2021-09-12	**Rev:**
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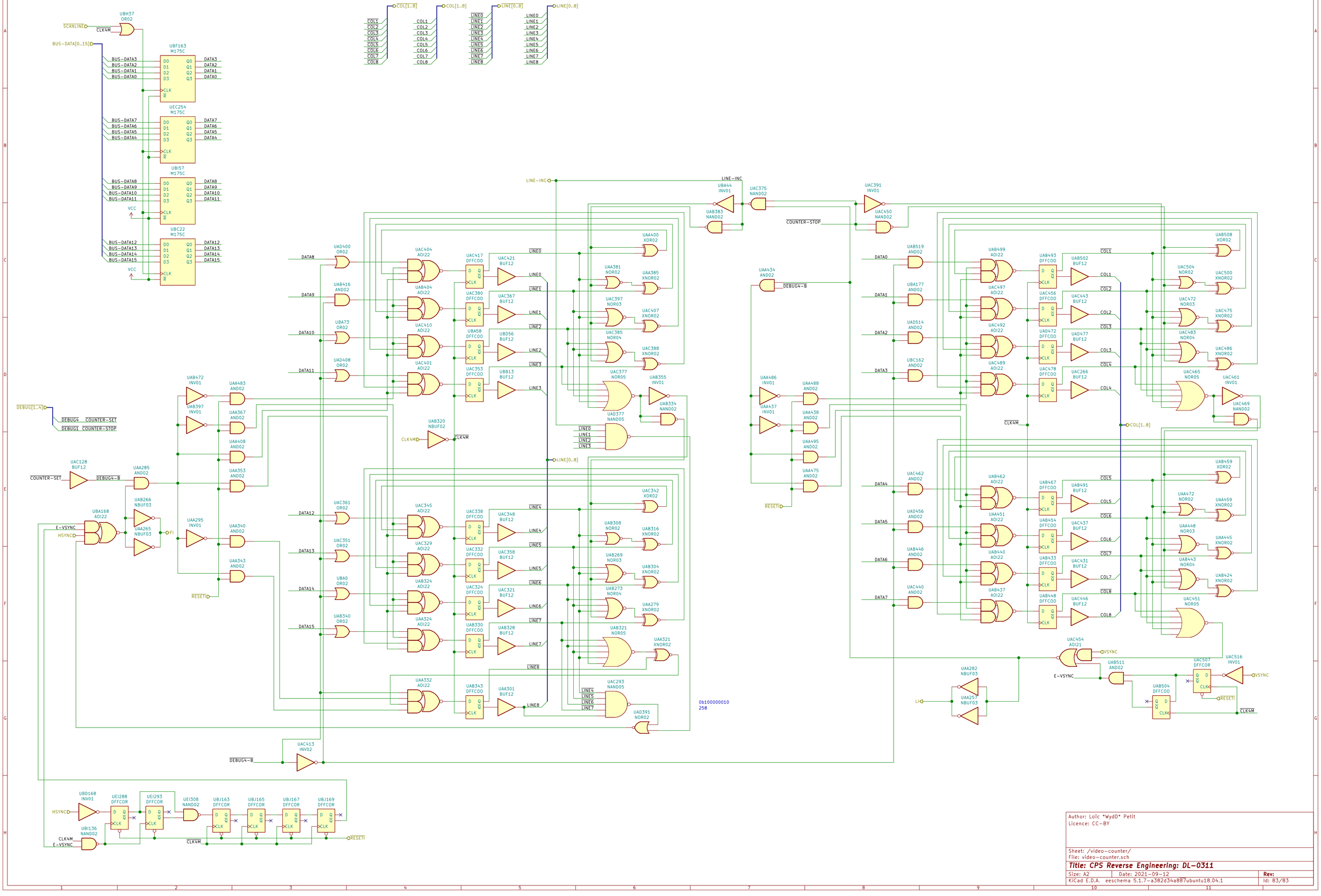
UBH37 OR02
SCANLINE
CLK4M
BUS-DATA[0..15]
UBF163 M175C
UEC254 M175C
UBI57 M175C
UBC22 M175C
BUS-DATA3
BUS-DATA2
BUS-DATA1
BUS-DATA0
BUS-DATA7
BUS-DATA6
BUS-DATA5
BUS-DATA4
BUS-DATA8
BUS-DATA9
BUS-DATA10
BUS-DATA11
BUS-DATA12
BUS-DATA13
BUS-DATA14
BUS-DATA15
VCC
DATA3
DATA2
DATA1
DATA0
DATA7
DATA6
DATA5
DATA4
DATA8
DATA9
DATA10
DATA11
DATA12
DATA13
DATA14
DATA15
COL[1..8]
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8
LINE[0..8]
LINE0
LINE1
LINE2
LINE3
LINE4
LINE5
LINE6
LINE7
LINE8
LINE-INC
UBA44 INV01
UAC375 NAND02
UAB383 NAND02
UAC391 INV01
UAC450 NAND02
COUNTER-STOP
UAA434 AND02
DEBUG4-B
UAB519 AND02
UBA177 AND02
UAD514 AND02
UBC162 AND02
UAC462 AND02
UAD456 AND02
UAB446 AND02
UAC440 AND02
UAD400 OR02
UAB416 AND02
UBA73 OR02
UAD408 OR02
UAC361 OR02
UAC351 OR02
UBA0 OR02
UAB340 OR02
UAC404 AOI22
UAB404 AOI22
UAC410 AOI22
UAC401 AOI22
UAC345 AOI22
UAC329 AOI22
UAB324 AOI22
UAA324 AOI22
UAA332 AOI22
UAC417 DFFC00
UAC380 DFFC00
UBA58 DFFC00
UAC353 DFFC00
UAC338 DFFC00
UAC332 DFFC00
UAC324 DFFC00
UAB330 DFFC00
UAB343 DFFC00
UAC421 BUF12
UAC367 BUF12
UBD56 BUF12
UBB13 BUF12
UAC348 BUF12
UAC358 BUF12
UAC321 BUF12
UAB328 BUF12
UAA301 BUF12
UAA381 NOR02
UAB385 NOR02
UAC397 NOR03
UAC385 NOR04
UAC377 NOR05
UAB269 NOR03
UAB273 NOR04
UAB321 NOR05
UAC293 NAND05
UAD391 NOR02
UAA400 XOR02
UAA385 XNOR02
UAC407 XNOR02
UAC388 XNOR02
UAB355 INV01
UAB334 NAND02
UAC342 XOR02
UAB308 NOR02
UAB316 XNOR02
UAB304 XNOR02
UAA279 XNOR02
UAA321 XNOR02
UAB320 NBUF02
UAB499 AOI22
UAB493 DFFC00
UAB502 BUF12
UAC497 AOI22
UAC456 DFFC00
UAC443 BUF12
UAC492 AOI22
UAD472 DFFC00
UAD477 BUF12
UAC489 AOI22
UAC478 DFFC00
UAC266 BUF12
UAB462 AOI22
UAB467 DFFC00
UAB491 BUF12
UAB451 AOI22
UAB454 DFFC00
UAC437 BUF12
UAB440 AOI22
UAB433 DFFC00
UAC431 BUF12
UAB437 AOI22
UAB448 DFFC00
UAC446 BUF12
UAB508 XOR02
UAC504 NOR02
UAC500 XNOR02
UAC472 NOR03
UAC475 XNOR02
UAC483 NOR04
UAC486 XNOR02
UAC465 NOR05
UAC461 INV01
UAC469 NAND02
UAA472 NOR02
UAA459 XNOR02
UAA448 NOR03
UAA445 XNOR02
UAB443 NOR04
UAB424 XNOR02
UAC451 NOR05
UAC454 AOI21
UAB511 AND02
UAA282 NBUF03
UAA257 NBUF03
UAC507 DFFC0R
UAC516 INV01
UAB504 DFFC00
VSYNC
RESETI
CLK4M
COL[1..8]
DEBUG[1..4]
DEBUG4 COUNTER-SET
DEBUG1 COUNTER-STOP
UAC128 BUF12
COUNTER-SET
UAA285 AND02
UBA168 AOI22
E-VSYNC
HSYNC
UAA265 NBUF03
FI
UAB266 NBUF03
UAA295 INV01
UAB472 INV01
UAB397 INV01
UAA483 AND02
UAA367 AND02
UAA408 AND02
UAA353 AND02
UAA340 AND02
UAA343 AND02
UAC413 INV02
UBD168 INV01
UEI288 DFFC0R
UEI293 DFFC0R
UEI308 NAND02
UBJ163 DFFC0R
UBJ165 DFFC0R
UBJ167 DFFC0R
UBJ169 DFFC0R
UBI136 NAND02
0b100000010
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